Network Communications
David Dietrich
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Replacement Sheet

Statement: This substitute Specification contains no new matter

Remarks:

- Page numbering, title, inventor, application number and identification as a substitute specification have been included in the header of each page.
- Paragraph numbering has been added.
- Entire document has been converted to 1.5 line spacing
- Footnotes have been removed and the text that they contained has been added to the body of the document
- Please disregard the paragraph number [0054], as this text is a continuation of paragraph [0053]
- Finally, because the markup version needed to have the edited content (footnotes) added back in to be shown as stricken, some of the page numbers may have shifted. The paragraph numbers will remain the same. Both documents will align in terms of page number starting at Appendix A.

NETWORK COMMUNICATION

[0001] CROSS REFERENCE TO RELATED APPLICATIONS

This application is related to U.S. Patent No. 5,390,181, granted on February 14, 1995, which is incorporated herein by reference in its entirety. This application is also related to U.S. Patent No. 6,278,713, granted on August 21, 2001, which is incorporated herein by reference in its entirety. This application is also related to U.S. Patent No. 6,292,493, granted on September 18, 2001, which is incorporated herein by reference in its entirety. This application is related to U.S. Patent No. 6,408,009, granted on June 18, 2002, which is incorporated herein by reference in its entirety.

[0002] FIELD

The present application relates to network communication.

[0003] BACKGROUND

Traditional Controller Area Network (CAN) protocol utilizes a Carrier Sense Multiple Access/Collision Avoidance (CSMA/CA) technique similar to that of Ethernet but with frames that are relatively small by networking standards in that the largest possible frame may be around 128-bits (i.e. 16-Bytes, including the maximum of 8-bytes for the payload), whereas the Ethernet Frame varies between 64-bytes and 1,536-bytes. Unlike Ethernet however, there is no loss of data as a result of collisions. This is because of CAN's unique non-destructive message arbitration methodology that guarantees high priority messages access to the CAN bus with no fear of collision or loss of data; hence, no need for retransmission.

[0004] However, the same feature that is CAN's strength (its non-destructive collision resolution methodology) is also its weakness in that as a CAN bus approaches its utilization capacity so does its propensity for indefinite starvation of lower priority messages. Given that a CAN message cannot arbitrarily change its priority; the CAN protocol is completely inflexible under heavy loads for successfully ensuring that lower-priority messages reach their destination. The traditional methodology as known in the art for resolving this problem has been in the separation of CAN nodes into multiple CAN sub-networks. However, such delineation can often be the source of frustration when attempting to discern the most efficient means for dividing the devices into disparate CAN networks while still affording cross network communication through various backhaul communication technologies. Embodiments presently disclosed provide security and reliability within a network, while maintaining CAN's distributed network communication methodology and implicit avoidance of single points of failure within the network.

[0005] BRIEF DESCRIPTION OF THE FIGURES

Figure 1 depicts an exemplary DQ Transmission Sequence;

Figure 2a and 2b depict an example of a Fully Loaded, Successful Transmission Sequence;

Figure 3 depicts an exemplary DQ Access Request Sequence Segment Structure;

Figure 4 depicts an exemplary DQ Mini-Slot (MS) Structure;

Figure 5 depicts an exemplary DQ Access Request Sequence Segment Structure with QoS Support;

Figure 6 depicts an exemplary Expanded (QoS Enabled) ARS Mini-Slot (MS) Structure;

Figure 7 depicts an exemplary ARS QoS Requested Message Priority Field;

Figure 8 depicts an exemplary DQ Node Network Address Field;

Figure 9 depicts an exemplary Complete DQ Frame Structure;

Figure 10 depicts an exemplary Standard Addressing DQ Frame Header;

Figure 11 depicts an exemplary Extended Addressing DQ Frame Header;

Figure 12 depicts an exemplary Basic DQ Packet Segment;

Figure 13 depicts an exemplary DQ Packet Segment Pre-Header Structure;

Figure 14 depicts an exemplary DQ Packet Segment Control Field;

Figure 15 depicts an exemplary DQ Fragmented Frame Header for the Initial Packet;

Figure 16 depicts an exemplary DQ Frame Header for the Initial Packet of a Resumed Frame Packet Sequence;

Figure 17 depicts an exemplary DQ Frame Header for a Resumed & Final Packet of a Frame;

Figure 18 depicts an exemplary Complete DQ Packet Overview of a Resumed & Final Packet of a Frame;

Figure 19 depicts an exemplary Complete DQ Packet Overview of the Final Packet of a Frame;

Figure 20 depicts an exemplary Complete DQ Packet & DQ Frame Overview of an Intermediate Packet of a Frame;

Figure 21 depicts an exemplary Overview of a Single DQ Packet containing a complete DQ Frame;

Figure 22 depicts an exemplary Packet Check Sequence (ONLY) within Packet Segment;

Figure 23 depicts an exemplary Basic DQ Packet Segment;

Figure 24 depicts an exemplary Management Information Command Field;

Figure 25 depicts an exemplary Message Check Sequence within Frame Segment;

Figure 26 depicts an exemplary Distribute DQSS Table Command Global Parameters;

Figure 27 depicts an exemplary Distribute DQSS Table Command Structure with Public Key Encryption;

Figure 28 depicts an exemplary Distribute DQSS Table Command Structure with Shared Key Encryption;

Figure 29 depicts an exemplary Distribute DQSS Table Command Structure with Encryption Disabled;

Figure 30 depicts an exemplary Distribute DQSS Table Command Node Record Parameters;

Figure 31 depicts an exemplary MI Disconnect Command Structure;

Figure 32 depicts an exemplary DQSS Management Segment Structure;

Figure 33 depicts an exemplary ARS Response from Cluster Head;

Figure 34 depicts an exemplary AP/CH ARS Mini-Slot Response Format;

Figure 35 depicts an exemplary embodiment according to the present application;

Figure 36 depicts an exemplary embodiment according to the present application;

Figure 37 depicts an exemplary embodiment according to the present application;

Figure 38 depicts an exemplary embodiment according to the present application;

Figure 39 depicts an exemplary embodiment according to the present application;

Figure 40 depicts an exemplary embodiment according to the present application;

Figure 41 depicts an exemplary embodiment according to the present application;

Figure 42 depicts an exemplary embodiment according to the present application.

[0006] In the following description, like reference numbers are used to identify like elements. Furthermore, the drawings are intended to illustrate major features of exemplary embodiments in a diagrammatic manner. The drawings are not intended to depict every feature of every implementation nor relative dimensions of the depicted elements, and are not drawn to scale.

[0007] DETAILED DESCRIPTION

In the following description, numerous specific details are set forth to clearly describe various specific embodiments disclosed herein. One skilled in the art, however, will understand that the presently claimed invention may be practiced without all of the specific details discussed below. In other instances, well known features have not been described so as not to obscure the invention. In addition, it should be understood that embodiments of the invention include both hardware and electronic components or modules that, for purposes of discussion, may be illustrated and described as if the majority of the components were implemented solely in hardware. However, one of ordinary skill in the art, and based on a reading of this detailed description, would recognize that, in at least one embodiment, the electronic based aspects of the invention may be implemented in software. As such, it should be noted that a plurality of hardware and software-based devices, as well as a plurality of different structural components may be utilized to implement the invention. Furthermore, and as described in subsequent

paragraphs, the specific mechanical configurations illustrated in the drawings are intended to exemplify

embodiments of the invention and that other alternative mechanical configurations are possible.

[0008] A Distributed Queuing Wireless Arbiter (DQWA) Protocol is based on the Distributed Queue Switch Architecture (DQSA) developed at the Illinois Institute of Technology. The DQSA was originally designed as Layers One (1) and Two (2) broadcast network architecture for cable TV networks that provided deterministic access to the transmission queue while simultaneously limiting collisions to a finite window within the DQ Transmission Frame. The DQSA may be extended into the wireless arena by focusing mostly on the Link Layer (i.e. Layer Two (2)) with only minimal direction regarding the Physical Layer (i.e. layer two (2)). The

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wireless nature of DQ may be defined in Distributed Queuing Wireless Arbiter (DQWA) with most of the specification dealing with the Link Layer while also providing only minimal direction for the Physical Layer.

[0008] The DQWA is a hybrid of a traditional "hub and spoke" network architecture with that of a peer-to-peer MESH network architecture. The primary area of focus of the DQWA specification is that of the Link Layer, although a key and critical aspect of it successful implementation, the Contention Window and associated Min-Slots, is heavily dependent upon the Physical Layer in that successful implementation of a unique Collision Detection mechanism may be implemented.

[0009] The heart of DQWA technology is a Medium Access Control (MAC) layer that allows an arbitrary number of stations to share a common communications channel over any distance and operating at any data rate. DQSA can operate over virtually any topology and will also provide a Quality of Service (QoS) at the MAC layer that includes the ability to temporarily elevate priorities in order to prevent starvation (as can occur in traditional CAN).

[0010] DQWA may be a distributed architecture with respect to communication. However, for control, DQWA is static for a given point in time; specifically, it is static for the duration of a DQ Transmission Frame. The designated central control point may transition to other nodes upon completion of the current DQ Transition Frame; which is why DQWA can be viewed as a hybrid between a pure MESH ad-hoc architecture and that of a traditional Hub-and-Spoke architecture.

[0011] The hybrid nature of the DQWA network architecture provides flexibility for adaptation to a CAN Wireless Extension in that communication is distributed while enabling a central authority to elevate priorities of messages as needed providing a QoS aspect to DQWA that CAN severely lacks. Also, because the central authority may shift from DQ node to DQ node if desired (i.e. enabled to do so), traffic patterns may be localized with respect to control. Thus, reducing latency when and where needed; according to the traffic pattern. Because all communication can be encrypted at the MAC layer, including the headers; security may be maintained at all times in spite of the fact that all traffic is broadcast wirelessly.

[0012] The key feature of DQSA is that all control resides in the stations, no central control is required. The network state is maintained at all times by each station in just two (2) binary counters per DQSS, providing it with all the information necessary to make decisions as to when to transmit for that specific DQSS. A DQ Transmission Frame may be divided into three separate time periods/segments listed below:

- 1) Referring to **Figure 35**, Contention Window (CW), utilized as part of the Access Request Sequence (ARS) **10** to the Transmission Queue with three (3) control mini-slots **15**, **20** and **25** acting as a finite sized Contention Queue;
- 2) Data and Control Window consisting of a single DQ Data and Control Frame; and,
- 3) Feedback Window, consisting of the DQ Feedback Frame with Synchronization Beacon.

[0013] A synchronization beacon may be transmitted to all stations prior to the start of each segment from which all stations must synchronize with for every transmission frame so that they may participate in the DQSS. The DQ Feedback Frame and associated Synchronization Beacon can come from any node within the DQSS, but is always sent by a single node at any given time and from which the node is typically chosen as one of a set of nodes designated for accessing gateways beyond the DQSS. Within a wireless environment, this central point would normally be referred to as the Base Station, Access Point, or Hub; the DQWA nomenclature for this central authority may be Cluster Head.

[0014] Variable length DQ Messages may be segmented into multiple data slots without requiring any further overhead. Qualities of Service (QoS) Priorities are available and it may be possible for a higher priority DQ Data & Control Frame to preempt a lower priority DQ Data & Control Frame during transmission within a period of one DQ Message. Segments may be allocated to a specific station thus providing time-division-multiplex (TDM) channels, commingled with normal DQ Frame traffic. The overall utilization within a wireless environment, i.e., ratio of data content to the channel capacity ranges from over 95% down to 80%;, depending upon frame size and overall network utilization.

[0015] As mentioned in above, because access to communication within a DQSS consists solely of member nodes, the entire contents within a MAC layer frame, including the header, may be encrypted; thus ensuring the both security and privacy. The purpose of the CW's ARS is twofold:

- 1. To afford current members of the DQSS with an opportunity to request communication privileges with one or more of the other nodes (including the Cluster Head) within the network; and
- 2. To simultaneously mitigate the potential for MAC & Data Payload collisions and hence, dropped frames resulting from corruption.

[0016] The latter is achieved by limiting the contention for access to the channel to a finite and predictable period of time. With the exception of the Cluster Head, all nodes may utilize this mechanism in order to access the MAC & Data Payload segment of the DQ Transmission Sequence. The ARS Segment **10** may be divided into three (3) sub-parts, termed, Mini-Slots (MS) **15**, **20** and **25** as shown in **Figure 35**.

[0017] The collision resolution process referenced above may utilize unique patterns transmitted by each soliciting device and a summation of those patterns in the event of a collision as a means for detecting collisions. The operation of DQWA is based on the m-ternary feedback information on the state of each of the mini-slots 15, 20 and 25. The Cluster Head may be able to distinguish between the three states: Idle, Success, and, Collision, for each mini-slot; as this information may provide protocol rules at the end of each frame. Each node may be assigned a unique bit pattern that has the property that when two or more ARS 10 collide, the pattern of the overlapping signal is distinguishable from the original pattern of any single ARS 10; hence, the Cluster Head can detect the collision.

[0018] In one exemplary embodiment, patterns are binomial coefficients; however, this number may be modified to meet the requirements of the targeted environment. Each node accepted into the network is assigned both a Node Address **30** and a constant size Code Word **35** of constant Hamming Weight as shown in **Figure 36**.

[0019] When a collision does occur, and particularly within an RF environment, it may be possible to determine that a collision has occurred since the collision may make the interpretation of the combined signal unintelligible. Further, even if the resultant collided signal does result in an intelligible result, the resulting Hamming Weight may be something other than the selected constant value. When taking into account that the correct associated DQSS node address must accompany the code word of constant hamming weight, the detection of a collision is possible.

[0020] DQWA may have an additional validation mechanism within the DQ Feedback Frame that protects against the unlikely occurrence of an illegitimate, but valid Code Word and DQSS Node Address combination resulting from a collision.

[0021] The aforementioned ternary decision described above may be subsequently determined as follows: Idle (i.e. no signal in ARS Mini-Slot) – Received Signal is below the RSSI (Noise) Threshold; Success – A demodulation resulting in the correct hamming weight and correct code word value and node address combination and again validated within the DQ Feedback Frame; Collision – Any signal detected above the noise (RSSI) threshold not resulting in a translation into the digital domain of a code word with the correct hamming weight and correct code word value and node address combination.

[0022] The Cluster Head may respond with the collision results as part of the DQSS Management Segment in order to clarify any potential ambiguities. Standard DQSS Network addresses may be 12-bits in length, with the lower 10-bits assigned for the dynamic portion of a valid address; as the upper two bits have special

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meaning. Both bits along with the rest of the DQSS Network Address are shown in **Figure 37**. Referring to **Figure 37**, a DQSS Node Cluster Bit **45** may be set to zero during the ARS.

[0023] The Most Significant Bit (MSB) of the address is reserved for the Cluster Head. This is particularly helpful if the Network Topology moves and the Cluster Head moves with it. Thus, allowing any node to maintain its original identity both before and after assuming the duties of the Cluster Head. In this way, the DQSS table maintains consistency regardless of which node is currently in charge of the network.

[0024] A DQSS Node Join Request Bit **45** may be used by nodes wishing to join the network. In order for an unknown node to be considered for admittance to the DQSS, it may be configured to satisfy the following two conditions:

- 1) The "Join Request" Bit 45 as shown in Figure 37 must be set within the DQSS Node Address Field. The Join Request Bit 45 allows for parts to be installed within a particular network architecture with little to any actual configuration in that "newly" installed parts can automatically request for inclusion in the desired vehicle's DQSS.
- 2) The "DQSS Mini-Cluster" Sub-Field 50 must set '7' (i.e. "111b").

[0025] The "DQSS Individual Address" Sub-Field **55** may be a value between '0' and "127" (i.e. a span of 128-values). The DQSS Mini-Cluster Sub-Field **50**, this is an important field in that it explicitly affords specific portions of a DQSS to be segmented into individual address spaces for the purpose of multi-cast addressing as well as enabling CAN sub-networks within a specific DQSS. The addition of a Message Bit to the DQSS Node Address Field (as alluded to in the previous section) would enable further enforcement of messages being restricted to specific CAN sub-networks.

[0026] The DQSS Individual Address Sub-Field **55**, these seven bits are used for assigning individual addresses, with any value between '0' and "126" assignable for an individual DQSS Network Address. The only time "127" may be used during the ARS is during a "Join Request." As "127" is otherwise set aside for "Directed Broadcasts" and regular "Broadcasts" for all Mini-Cluster Sub-Field values except for '7' (i.e."111b").

[0027] A key component of the DQ Service Set concept is network security and the rules by which nodes may become members of a specific DQ Service Set. A DQSS can operate in one of three operational modes listed below the operational modes listed in decreasing order of centralized membership control: Static Association Mode; Semi-Manual Association Mode; Promiscuous Mode. Each of the modes will now be individually discussed in detail.

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[0028] In Static Association Mode, the DQSS is completely pre-configured. New nodes may not request to join and can only become part of the DQSS either by directly adding nodes to an existing DQSS Configuration Database or by installing a completely new DQSS Configuration Database containing the desired nodes. In response to the fact that a DQSS configured in Static Association Mode cannot add nodes in real time (doing so onlythrough configuration); any attempt to submit a DQSS Membership Request Code Word during the ARS segment will be ignored.

[0029] A DQSS configured to be in Semi-Manual Mode has all of the capabilities of a Static Association Mode DQSS as well as the additional ability to add nodes in real time. There are two methods for which a node may acquire inclusion within a DQSS configured in DQ Semi-Manual Association Mode. The first method for acceptance for a given node into a DQSS while in DQSS Semi-Manual Association Mode is via manual configuration as part of a DQSS Configuration Database. The second method utilizes a two-step process for any node outside of the current DQSS membership and described below:

- 1) First, the Candidate Node must issue a request for DQSS Inclusion.
- 2) Second, an external confirmation of the request from either an operator (i.e.service technician or factory installation personnel) or configuration robot utility must explicitly accept the Candidate Node into the DQSS; presumably based upon some criteria established for admission.

[0030] It is the latter act that serves as the basis for the moniker, "DQSS Semi-Manual Association Mode" since confirmation of inclusion requires an explicit action from an external source.

[0031] A DQSS configured to be in Promiscuous Association Mode has two methods for DQSS membership inclusion. As with all modes, the first method for inclusion into a DQSS is through configuration. The second method for inclusion into an existing DQSS is similar to the second inclusion method listed for DQSS Semi-Manual Association Mode; however, no operator intervention is required except for the case of an operator explicitly desiring to exclude a node from the DQSS.

[0032] Thus, the only time external intervention occurs during a DQSS operating in Promiscuous Association Mode is when an operator wishes to explicitly "blacklist" a candidate node; adding it to either a permanent blacklist or a blacklist that can be aged out. An example of a situation in which permanent blacklisting may be desired would be if a paid subscriber for XM Radio or other paid electronic subscription service was delinquent in paying their subscriber fees and/or had exceeded their usage. The subscriber could then be explicitly blacklisted until they brought their account current again and/or purchases additional time. An example of temporary blacklisting could occur as a result of a background task monitoring network usage. If there was a limit as to the daily network activity for a particular subscriber and that subscriber had exceeded their limit, the Candidate Node of the subscriber could be placed on a blacklist that expired whenever their

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"lease" renewed again. While there are certainly other, potentially more cogent examples, each of the above examples sufficiently illustrates the viability of the blacklist exclusion capability.

[0033] Encryption may be used in any mode and can be implemented such that there is little, if any affect, as to how each Association Mode operates. There are two different types of encryption used within DQWA: Encrypted Private Key Mode; and Encrypted Public Key Mode. Both of these encryption methodologies will now be discussed in relation to their effects on operating modes. A DQSS configured to be in Encrypted Private Key Mode utilizes a symmetric encryption methodology with respect to both encrypting outgoing messages and decrypting incoming messages. Because both sides know what the decryption algorithm is, both sides may transmit the entire message encrypted, including the header. The clear implication with this mode is that the encryption/decryption algorithms must be done within the PHY in hardware in order for the three operating modes (Static, Semi-Manual, and Promiscuous) to operate oblivious to the effects of encryption performed on the encapsulated data.

[0034] A DQSS configured to be in Encrypted Public Key Mode utilizes an asymmetric encryption methodology with respect to the encryption of outgoing messages and decrypting incoming messages. Specifically, the shared (i.e. private) key is used for decrypting messages, but the public key must be utilized for encrypting messages. In this way, the entire message may be encrypted (as is done with Private (Shared) Key Mode), but the public key must be known in order to encrypt an outgoing message. Thus, nodes wishing to "join" the network, regardless of the configuration must "listen" to the Feedback Packet in order to get the Public Key before they can transmit. The cogent point here is that although the public key is broadcast, it is done so in encrypted form using the "Private" key; thus adding an additional layer of security to this process.

[0035] One of the advantages to this encryption mode to the automotive industry is that the public key could be provided to all legitimate parts vendors without sacrifice of security. The designated Cluster Head within a specific vehicle could then validate the part as valid or invalid according to the default configuration within the vehicle database. Not only would this serve the purpose of providing security to the vehicle insofar as normal traffic is concerned, it also ensures that only authorized parts may be used for a given vehicle type.

[0036] DQ supports Dynamic Clustering for the Control Point of DQ Network Topology. If Dynamic Clustering is disabled, the Cluster Head serves as the static control point of the vehicle DQSS network. Thus, if the static DQSS Cluster Head goes down, so does the DQ Network. However, if Dynamic Clustering is enabled, the Dynamic Cluster Head Designation Order will be included within the DQSS and updated separately on a periodic basis. There are multiple events that may trigger a Cluster Head Transition including traffic loading, hardware and/or power failures, energy consumption fairness criteria, or simply user discretion are a few of the more prominent events. Therefore, in order to support the various types of event triggers,

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there are multiple selections for the type of Cluster Topology configuration. The different Cluster Topology configuration types are listed below:

- **Clustering Disabled** The network is complete static, with one and only one node designated as the central control and arbitration point. Thus, if the Cluster Head fails, then the overall network connectivity also fails.
- Clustering Enabled for Backup Only So long as the network is operating normally, the network is completely static; with a single node designated as the Cluster Head. However, in the event the designated Cluster Head fails, a succession of backup Cluster Heads have been previously identified within the DQSS Table and thus assume the role of the Cluster Head according to their priority order and online status (i.e. the node that is both "online" and has the highest designated priority status becomes the Cluster Head if the current Cluster Head fails; if the highest designated priority status node is not online then the duty falls to the next lower designated priority status node). In the event there are no nodes that are online and have been designated as a backup Cluster Head, the network connectivity fails.
- **Limited Clustering Enabled** Normal Clustering is enabled for the network with this setting; however, only a limited set of designated nodes may participate as Cluster Heads.
- **Clustering Enabled** Normal Clustering is enabled for the network, with all nodes eligible for Cluster Head designation.

[0037] As alluded to above, for clustering to occur within a DQSS not only must the overall Cluster Topology be specified, but so must the Clustering Methodology.

[0038] At present there are three distinct Clustering Methodologies: 1. Static Clustering; 2. Traffic Flow Clustering; and 3. Traffic Flow with Topology Coverage Clustering.

1) Static Clustering

Regardless of the setting of the Cluster Topology for a given DQSS, if the Cluster Methodology is set to "Static Clustering", then Dynamic Cluster is completely disabled. This is the only setting allowed for the "Clustering Disabled" and "Clustering Enabled for Backup Only" Cluster Topologies. If this setting is used for either the "Limited Clustering Enabled" or "Clustering Enabled" topologies, then the net effect is to force the overall network topology into that of "Clustering Enabled for Backup Only".

2) Traffic Flow Clustering

Traffic Flow Clustering enables the Cluster Head to be located at the node providing the most efficiency with respect to being a "gate keeper" of the traffic flow. Because all communication and control is distributed and is not routed through a central spoke in order to communicate with other nodes within the DQSS, the only real advantage to the Cluster Head moving as the flow moves would be if the gateway

can move with it. Meaning, the Cluster Head nodes have dual functionality with one port servicing the DQSS and other ports servicing one or more gateways.

3) Traffic Flow with Topology Coverage Clustering

Traffic Flow with Topology Coverage Clustering enables the Cluster Head to be located at the node providing the greatest coverage for the current traffic flow. The distinction between this mode and standard "Traffic Flow Clustering" is that the former does not take into account the overall range of coverage of the client nodes within the DQSS.

[0039] Similar to standard "Traffic Flow Clustering", because all communication and control is distributed and is not routed through a central spoke in order to communicate with other nodes within the DQSS, the only real advantage to the Cluster Head moving as the flow moves would be if the gateway can move with it. Thus, as above, in order for this mode to be effective, Cluster Head nodes must have dual functionality with one port servicing the DQSS and other ports servicing one or more gateways. The Cluster Head distributes the DQSS table on a periodic basis. No node may communicate with another node unless both nodes are contained within the same DQSS.

[0040] Because of the strict adherence to this policy, in order for a node to join and subsequently communicate with other nodes, including the Cluster Head, within the DQSS, the following sequence of events may occur:

- a) The Cluster Head may explicitly acknowledge and admit a node for inclusion into the DQSS;
- b) The Cluster Head may then add it to the DQSS and perform either a complete or partial DQSS update of the DQSS Table to the nodes within the DQSS.

[0041] The Cluster Head may first admit the node in the network and then secondarily inform the other nodes in the DQSS of the joining node's admission into the DQSS. The format of the DQSS Table includes the following:

- DQSS Configuration Data; providing information specifying the functional and operational makeup of the DQSS. Information included would be the DQSS Mode (i.e. Static, Manual, Promiscuous, Promiscuous-Shared Key), Encryption Indication, DQ Gateway Information, Maximum DQ Frame and DQ Packet Sizes;
- 48-Bit MAC Address of every Node within the DQSS;
- 3) 12-Bit DQSS Address; this address is assigned by the Cluster Head to the individual nodes within the DQSS as a means of reducing the amount of overhead within the transmission stream;
- 4) Static Sized Code Word, assigned by the Cluster Head, and used for Access Requests to the Transmission Queue. This value is coupled with the DQSS Address on all access requests;
- 5) Active or Inactive Indicators for Every DQ Member.

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[0042] Given that the primary purpose of the DQSS Table is to maintain the integrity of the network, a DQSS Table should be viewed as an Object Oriented Encapsulation of a specific DQ Network.

[0043] The bandwidth in DQWA may be divided into fixed-size segments and groups of contiguous segments are allocated to each DQ Frame but many applications, such as a fuel injection module would be better served with the equivalent of a TDM channel. DQWA supports this feature; a node requests that a segment be allocated on a recurring basis resulting in an isochronous (TDM) channel of the desired bandwidth. This feature is of true significance since it means that DQWA can satisfy with equal facility both packet and fixed-bandwidth requirements.

[0044] Each DQ Data & Control Frame contains the total number of bytes within the frame at the beginning of the header; thus non-essential devices may go into a power save sleep mode for the period of the DQ Data & Control Frame transmission; awaking in time for the DQ Feedback Frame and inclusive DQ Transmission Beacon.

[0045] There is no congestion in a DQSA network thus networks may be designed for average loading of 90%. The surges over 100% that cause chaos in conventional routers just mean that the distributed queues get longer, temporarily.

[0046] There are no lost packets except for those lost due to Line Error. If only a single node has packets to send, that node can utilize 100% of the available capacity, when a second node desires to transmit, the available capacity is split automatically without any central control input, evenly between the two stations. And so on for an arbitrary number of stations. Priorities can be utilized to negate this inherent fairness.

[0047] The distributive and non-static control aspect of DQWA affords DQWA to be used "As Is" within environments requiring mission critical and/or fail-safe architectures and without any additional redundancies in the network. Unlike conventional Hub-and-Spoke architectures, the current DQWA control node within a given DQWA network may fail without affecting the communication abilities of the remaining nodes within the DQSA network. In short, DQWA eliminates the single point of failure, which is common in all commercial network architectures deployed today. This is huge benefit that Mission and Safety Critical applications a built-in mechanism within the network architecture for supporting their specific application. A DQWA network becomes part of the Mission and/or Safety Critical Solution and not another problem for which a work-around must be found (usually involving duplicate and/or alternative hardware and communication paths).

[0048] The distributive and non-static (i.e. transitional) control aspect of DQWA affords DQWA to be used "As Is" within environments requiring mission critical and/or fail-safe architectures (like that necessitated

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within the automotive domain) and without any additional redundancies in the network. Further, given the increasing security needs of automotive onboard network devices and the ubiquitous and pervasive nature of CAN; DQWA would be an excellent complimentary technology for wireless CAN networks; particularly as a wireless CAN backhaul topology.

[0049] Distributed Queuing Wireless Arbiter (DQWA)

Referring to **Figures 38** and **39**, DQWA is a broadcast medium MAC Layer Protocol and PHY Interface that is carrier independent and is specifically designed to be a wireless back-haul solution for the transportation of both mobile telephony data and TCP/IP network data.

[0050] DQWA may provide the following advantages over the systems known in the art:

- 1) Non-LoS Support (requires Dual Antenna)
- 2) Increased Bandwidth Utilization bandwidth efficiency up to 95%.
- 3) Organic Network Organization (capability to assemble and grow automatically)
- 4) Built-in Redundancy of Network Control Mechanisms
- 5) Direct Peer-to-Peer communication for nodes within same service set (i.e. local network); meaning no retransmission by central control required.
- 6) Built-in capability for energy efficiency.
- 7) No physical network size restriction (can be adapted for any number of nodes).
- 8) Carrier and Modulation independent designed for adaptation to virtually any carrier, modulation, and data rate.

[0051] Referring to **Figures 40** and **41**, DQWA may allow backhaul providers to quickly augment existing infrastructure with equipment that is easy to install and configure (self-configuring if enabled) while being more efficient than other comparable solutions (such as Wi-Max).

[0052] DQWA Backhaul Technology may be an alternative to both traditional Point-to-Point (P2P) backhaul and Star Topology solutions. With a DQWA system, the data moving between a Micro-cell Aggregation Point (termed, Cluster Node) and the Macro Cell Aggregation Point (termed, Cluster Head Node) may pass through a neighbor Micro-cell Aggregation Point before reaching the Macro Cell Aggregation Point. This 'multi-hop' function provides an extended array of data routing options to overcome LoS restrictions from that of a traditional P2P or even Star Topology Solution.

[0053] The advantages of a DQWA backhaul solution are numerous and sizable. Of primary importance is the potential ability to deploy Pico-cells wherever and however the carrier desires without concern for LoS limitations or fiber/copper run cost considerations. With Siting and backhaul comprising the large majority of

[0054] Pico-cell deployment costs, DQWA may bring a key CAPEX reduction to the operator. DQWA systems may reduce the average RF link distances; hence reducing the radio & antenna costs and further reducing backhaul CAPEX. And as DQWA systems select the 'best-path' route, network reliability is increased and OPEX is reduced. Reliability may also be gained through the flexible nature of DQWA as a result of the fact that the Micro Cell Base Station does not need to be a single fixed node and may in fact transition from node to node within the Pico-Cell. Thus, allowing automatic recovery if the primary Micro Cell Base Station should fail.

[0055] Figure 42 depicts an exemplary embodiment of DQ Transmission sequence according to the present application.

DQWA - Common Terms:

Access Request Sequence (ARS) – The ARS occurs within the Contention Window Segment and consists of three mini-slots within the segment acting as elements of the Contention Queue.

Cluster Head – The Cluster Head is the central and only arbiter for a specific DQSS.

Cluster Head Master – The preferred Cluster Head within a given DQSS.

Cluster Head Priority - The predefined priority of nodes that may assume the role as Cluster Head.

Cluster Node – Any node within the DQSS that is NOT the Cluster Head.

Contention Queue - FIFO Queue used by DQSS for candidacy into Transmission Queue.

Contention Window Segment – The Cluster Head is the central and only arbiter for a specific DQSS.

Distributed Queuing Service Set (DQSS) – Collection of nodes that are defined to be within a specific DQ Network.

DQ Payload & Control Packet Segment – This segment encapsulates Data and optional Control Information.

Feedback Packet (FBP) Segment – This segment encapsulates Data and optional Control Information from the Cluster Head and serves as a Transmission Beacon for the DQSS.

Transmission Queue – FIFO Queue with Optional Priorities used by DQSS to maintain order of scheduled transmissions.

Transmission Sequence – Term describing the complete sequence of the standard periodic transmission that occurs within a DQSS network. The Transmission Sequence is delineated into three separate and contiguous segments (listed below in the order of their appearance):

Contention Window Segment

Payload & Control Packet Segment

Feedback Packet Segment

ARS Contention Window – Refers to the period of time within the DQ Transmission Sequence in which nodes may contend for access to the DQ Transmission Queue.

- ARS Mini-Slot Refers to the period of time within the DQ Transmission Sequence in which nodes may contend for access to the DQ Transmission Queue.
- DQSS ARS Segment Refers to the first segment within the DQ Transmission Sequence, which is when nodes may request access to the DQSS' Transmission Queue.
- DQSS Feedback Packet Segment Refers to third and final segment within the Transmission Sequence, which is where the node acting as the Cluster Head provides feedback to the nodes within the DQSS. This is also where it may preempt both ongoing transmissions as well as upcoming and previously scheduled transmissions in favor of higher priority transmissions.
- DQ Frame Refers to collection of one or more DQ Control and Payload Packets; when application data is included within the collection of packets, the DQ Frame represents a single complete logical unit of encapsulated application data.
- DQ Control and Data Payload Packet Segment Refers to the middle segment within the DQWA Transmission Sequence. This segment can carry both control and payload information within.
- DQ Segment Refers to one of three logically distinct delineations within a DQ Transmission Sequence (listed as follows):

Access Request Sequence Segment;

DQ Control and Payload Packet Segment;

Feedback Packet Segment.

- DQ Service Set (DQSS) Refers to a set of nodes within a DQ Network that share a common peerto-peer communication medium and are managed by a single authority that utilizes queues to control access to the DQ Network.
- DQ Transmission Sequence Refers the complete sequence of the three DQ Segments (i.e. ARS, Payload, Feedback) repeatedly, consistently, and always occurring in every DQWA transmission.
- Feedback Window Refers to the period of time within the DQ Transmission Sequence in which the Access Point or Cluster Head provides feedback to the nodes within the DQSS.
- Queue Transmission Window Refers to the period of time within the DQ Transmission Sequence in which the node at the top of the Transmission Queue is afforded the opportunity to transmit.

ACK Acknowledgment

ACK_AL Acknowledgment in Active Listening

AL Active Listening
AP Access Point

ARQ Automatic Retransmission/Repeat Request

ARS Access Request Sequence
BEB Binary Exponential Back-off

C-ARQ Cooperative ARQ

CCA Clear Channel Assessment

CDMA Code Division Multiple Access

CFC Call for Cooperation

CRC Cyclic Redundancy Code
CRQ Collision Resolution Queue

CSMA Carrier Sensing Multiple Access

CSMA/CA Carrier Sensing Multiple Access with Collision Avoidance

CTS Clear to Send

DBE Detailed Balance Equations

DCF Distributed Coordination Function

DIFS DCF Inter Frame Space

DPCF Distributed Point Coordination Function

DQ Distributed Queuing

DQCOOP DQMAN for Cooperative ARQ

DQMAN Distributed Queuing MAC protocol for Ad Hoc Networks

DQWA Distributed Queue Wireless Arbiter
DSSS Direct Sequence Spread Spectrum

DTQ Data Transmission Queue

ED Error Detection

FBP Feed-Back Packet

FCS Frame Check Sequence
FEC Forward Error Correction
GUI Graphic User Interface

IMSI Initial Master Sensing Interval

IEEE Institute of Electrical and Electronics Engineers

ISM Industrial, Scientific, and Medical free-license band

ISO International Standards Organization

LAN Local Area Network

MAC Medium Access Control

MACSWIN The MAC Simulator for Wireless Networks

MCR Master Cooperation Request
MCS Message Check Sequence
MIFS Maximum Inter Frame Space
MIMO Multiple Input Multiple Output
MRAC Multiple Relay Access Control

MSP Master Selection Phase

MSS Master Service Set

MSSI Master Sensing Selection Interval

MTO Master Time-Out

NAV Network Allocation Vector

OSI Open System Interconnection

PAN Personal Area Network

PCF Point Coordination Function

PDA Personal Digital Agenda

PLCP PHY Layer Convergence Procedure

PHY Physical Layer

PIFS PCF Inter Frame Space

QoS Quality of Service RTS Request to Send

SIFS Short Inter Frame Space

SNIR Signal to Noise plus Interference Ratio

SNR Signal to Noise Ratio STC Space-Time Codes

TDMA Time Division Multiple Access

WLAN Wireless LAN

WWRF Wireless World Research Forum

[0056] Automotive Industry:

In one exemplary embodiment, the DQWA may be applied in the automotive industry. The DQWA is ideal for applications requiring distributed communication and control, of which the automotive world certainly falls into that category. In short, DQWA adds the ability to simplify intra-vehicle connectivity while expanding overall communication capabilities.

[0057] The CAN protocol has served the automotive and related industries well for over twenty-five (25) years; with the original CAN protocol officially released in 1986 followed by the release of CAN 2.0 in 1991. Since then many variants and improvements in CAN combined with the proliferation of automotive onboard microprocessor based sensors and controllers have resulted in CAN establishing itself as the dominant network architecture for automotive onboard communication in layers one (1) and two (2). Going forward however, the almost exponential growth of automotive onboard computing and the associated devices necessary for supporting said growth will unfortunately necessitate an equivalent growth in the already crowded wired physical infrastructure unless a suitable wireless alternative can be provided.

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[0058] While a wireless implementation of CAN has been produced, it has never obtained real traction within the automotive world. Other alternative methodologies for providing wireless connectivity have been much more pervasive and accepted, but none of them provide anything more to CAN interfaces than a CAN-to-Wireless Bridge; with Wi-Fi, Blue Tooth, and GSM being the primary wireless network architectures bridging to CAN.

[0059] Contrary to prior art, present application provides more than simply a wireless extension of CAN in that it does more than extend CAN into the wireless domain (as was the case with CANRF). As pure wireless CAN with no accommodations for heavy utilization would only exacerbate CAN's primary deficiency of starving out lower priority messages; since there would be no way to isolate devices in sub-networks as could be done with a wired infrastructure.

[0060] Embodiment presently disclosed remove CAN's deficiency by modifying the newly defined wireless network protocol and architecture, DQWA (Distributed Queuing Wireless Arbiter) to not only extend CAN into the wireless domain, but also addresses CAN's more prominent shortcomings.

[0061] Recognizing the proliferation of devices with network connectivity within vehicles is going to continue escalating; it is logical to look for a means to facilitate this expansion without an equivalent expansion in wired infrastructure. Anyone who has looked under the hood of a vehicle from the 70's and then compared that to what is under the hood today must wonder where the space for any additional infrastructure is going to come from.

[0062] The same is true for under the dashboard and/or in the trunk with respect to entertainment systems. Consumers want more space, not less; they want their technologic advances without paying the price in either comfort or cost. The only foreseeable path to that end is a wireless one. It is this path that brings fewer wires; lower costs; easier installation; greater capabilities for expansion. DQWA is a solution that provides both security and reliability within a wireless framework, while maintaining CAN's distributed network communication methodology and implicit avoidance of single points of failure within the network.

[0063] Given the proliferation of network devices in people's daily lives, it is only logical to deduce a similar growth pattern within vehicles. As that growth pattern continues, it will become increasingly difficult to depend so heavily on a wired infrastructure for providing communication connectivity within the vehicle. Of greater significance will be the proliferation of automotive onboard devices that will be expected to communicate externally; particularly with respect to both personal data derived from the human passengers as well as vehicular data exchanged with vehicular traffic management technology both fixed and potentially with other

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vehicles. It is clear for many reasons, both because of the physical limitations, difficulty, and expense of installing and maintaining wired bus infrastructures that the necessity of a wireless alternative is inevitable.

[0064] The primary weakness in attempting to utilize CAN within a heavily utilized bus is the propensity for lower priority messages to be starved out and hence never sent; or sent too late to be of any use. Obviously, if CAN is to be deployed within a wireless environment then this weakness becomes a severe problem given that it will become difficult for CAN nodes to form a sub-network within the same vehicle; not to mention potential interference from external sources, including CAN nodes broadcasting on the same frequency in nearby vehicles. Even if adequate RF shielding and filtering techniques are utilized within the vehicle chassis to maintain successful RF communication; given the limited number of available frequencies, a methodology would still need to be employed that would facilitate coexistence with other nodes broadcasting on the same frequency within the vehicle; particularly with respect to access to the bus' transmission queue. Also, given the real-time, mission and safety critical nature of automotive communication, reliability and robustness must be key considerations in any deployed networking methodology supporting automotive communication.

[0065] Given that by definition wireless communication is ubiquitously broadcast, security becomes a crucial concern. Examples of such concern consists both of those from listening in violating both privacy and network security as well as those attempting to gain unwanted access over the network devices within the network (ex. either by either directly manipulation of the devices or by indirect manipulation via the spoofing of existing devices within the network). Additionally, as more and more automotive modules require intra-vehicle network connectivity, wireless becomes the only viable alternative. The challenge is to enable the transition to wireless connectivity, reliably, safely, and most of all securely. DQWA provides the answer to this increasingly important and difficult problem.

[0066] An exemplary Distributed Queuing Wireless Arbiter (DQWA) PHY and MAC Protocol Specification according to the present application is provided next.

"DISTRIBUTED QUEUING WIRELESS ARBITER (DQWA) PHY & MAC PROTOCOL SPECIFICATION"

[0067] 1.0 Objective and Scope

The philosophical premise of this document is to take the DQ Protocol MAC & PHY beyond the theoretical realm and move it squarely into the application and development reality. Resulting from that directive, there are two stated primary objectives for this document.

[0068] 1.1 Define the Distributed Queuing Wireless Arbiter (DQWA) Protocol

The first objective is to describe and specify the DQWA Protocol MAC & PHY in sufficient enough detail so that any two implementations resulting from the aforementioned specification are 100% interoperable. In fulfilling the first objective, much of this document is spent in fully defining the DQWA Protocol.

[0069] While DQWA is designed to outperform most, if not all, current wireless environments including 802.11 based technologies; particular attention is given to honing the DQWA protocol for its initial target market as a Wireless Mobil Backhaul Technology primarily servicing countries without significant copper and/or fiber communication infrastructure. It is with that in mind that the first full draft of DQWA has been designed.

[0070] Additionally, the reader will note that while Wireless Mobile Backhaul is the primary target, DQWA also has features specifically designed in to work with and as a replacement for mobile last mile solutions. The premise of such thinking is that deploying a technology that can be used across a broad spectrum of applications (i.e. mobile backbone, last mile, and even WLAN if desired) means lower cost, easier deployment, and greater bandwidth.

[0071] Lastly, so much of the world is moving towards automating environments that require mission and/or safety critical applications. It just so happens that the primary concern within these environments is eliminating single points of failure. Whenever a network is involved in such an environment, the only mechanism for achieving that is duplication. Fortunately, because the Cluster Head within a DQWA Network can move, with any node being capable of assuming Cluster Head responsibilities; very little needed to be added in order to take advantage and utilize the distributive nature of the DQWA network for this purpose.

[0072] 1.2 Provide Technology Plan and Associated Implementation Outline

The first objective is to provide a Technology Plan and associated Implementation Schedule outline that:

- Specify the individual features to be implemented.
- Specify the implementation order of those features.
- Specify which features are not covered within the scope of this document.
- Specify the future direction of the DQWA MAC & PHY Technology.

[0073] 1.3 Objective and Scope Conclusion

The second objective is to provide a Technology Plan and associated Implementation. The expectation of achieving both stated objectives (i.e. defining the protocol and Technology Plan) will enable consistency for both implementers and users alike.

[0074] 2.0 Background and Related Information

The Distributed Queuing Wireless Arbiter (DQWA) Protocol is based on the Distributed Queue Switch Architecture (DQSA) developed at the Illinois Institute of Technology. The heart of this technology is a medium access control (MAC) that allows an arbitrary number of stations to share a common communications channel over any distance and operating at any data rate. DQSA can operate over virtually any topology and will also provide a Quality of Service (QoS) superior to any currently available.

[0075] The key feature of DQSA is that all control resides in the stations, no central control is required. The network state is maintained at all times by each station in just two (2) binary counters per DQ Service Set (DQSS), providing it with all the information necessary to make decisions as to when to transmit for that specific DQSS. A DQ Transmission Frame is divided into three separate time periods or segments; with the three segments listed below:

- 1) Contention Window, utilized as part of the Access Request Sequence (ARS) to the Transmission Queue with three (3) control mini-slots acting as a finite sized Contention Queue;
- 2) Data and Control Window consisting of a single DQ Data and Control Frame; and,
- 3) Feedback Window, consisting of the DQ Feedback Frame with Synchronization Beacon.

[0076] The only "central" control required is that a synchronization beacon must be transmitted to all stations prior to the start of each segment from which all stations must synchronize with for every transmission frame so that they may participate in the DQSS. The Feedback Packet and associated Synchronization Beacon can come from any node within the DQSS, but is always sent by a single node at any given time and from which the node is typically chosen as one of a set of nodes designated for accessing gateways beyond the DQSS. Within a wireless environment, this central point would normally be referred to as the Base Station, Access Point, or Hub.

[0077] Variable length packets may be segmented into multiple data slots without requiring any further overhead. Qualities of Service (QoS) Priorities are available and it is possible for a higher priority packet to preempt a lower priority packet during transmission within a period of one Transmission Sequence.

[0078] Segments can be allocated to a specific station thus providing time-division-multiplex (TDM) channels, commingled with packet traffic. The overall utilization within a wireless environment, i.e., ratio of data slot content to capacity of channel will rangefrom over 95% down to 80%, depending upon frame size and overall network utilization.

[0079] Lastly, because access to communication within a DQSA service set consists solely of member nodes, the entire contents within a MAC layer frame, including the header, may be encrypted; thus ensuring the utmost of both security and privacy.

[0080] In addition to the original work done by Graham Campbell, Ph.D., as referenced in [1] and [2], acknowledgements and credit should be given to Luis Alonso, PhD, Jesús Alonso Zárate, PhD, and their research team at the Polytechnic University of Catalonia, Spain. In addition to heavy dependence on their many papers, many of which are published by the IEEE; they have also provided a significant amount of time, feedback, and guidance in defining the DQWA Protocol discussed and detailed within this document. Thus, while every instance is not cited, all relevant documents used as research material have been cited within the index section of this document; with much attention given to the documents directly focused on the protocol, Distributed Queuing with Collision Avoidance (DQCA) (i.e. [4], [5]).

[0081] 3.0 Glossary of Terms and Acronyms

3.1 Acronyms

ACK Acknowledgment

ACK_AL Acknowledgment in Active Listening

AL Active Listening
AP Access Point

ARQ Automatic Retransmission/Repeat Request

ARS Access Request Sequence
BEB Binary Exponential Back-off

C-ARQ Cooperative ARQ

CCA Clear Channel Assessment
CDMA Code Division Multiple Access

CFC Call for Cooperation

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ED Error Detection

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GUI Graphic User Interface

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IEEE Institute of Electrical and Electronics Engineers

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LAN Local Area Network

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MACSWIN The MAC Simulator for Wireless Networks

MCR Master Cooperation Request
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MIFS Maximum Inter Frame Space
MIMO Multiple Input Multiple Output
MRAC Multiple Relay Access Control

MSP Master Selection Phase

MSS Master Service Set

MSSI Master Sensing Selection Interval

MTO Master Time-Out

NAV Network Allocation Vector
OSI Open System Interconnection

PAN Personal Area Network

PCF Point Coordination Function
PDA Personal Digital Agenda

PLCP PHY Layer Convergence Procedure

PHY Physical Layer

PIFS PCF Inter Frame Space

QoS Quality of Service
RTS Request to Send

SIFS Short Inter Frame Space

SNIR Signal to Noise plus Interference Ratio

SNR Signal to Noise Ratio
STC S pace-Time Codes

TDMA Time Division Multiple Access

WLAN Wireless LAN

WWRF Wireless World Research Forum

[0082] 3.2 Terms

ARS Contention Window – Refers to the period of time within the DQ Transmission Sequence in which nodes may contend for access to the DQ Transmission Queue.

ARS Mini-Slot – Refers to the period of time within the DQ Transmission Sequence in which nodes may contend for access to the DQ Transmission Queue.

- **DQSS ARS Segment** Refers to the first segment within the DQ Transmission Sequence, which is when nodes may request access to the DQSS' Transmission Queue.
- **DQSSFeedback Packet Segment** Refers to third and final segment within the Transmission Sequence, which is where the node acting as the Cluster Head provides feedback to the nodes within the DQSS. This is also where it may preempt both ongoing transmissions as well as upcoming and previously scheduled transmissions in favor of higher priority transmissions.
- **DQ Frame** Refers to collection of one or more DQ Control and Payload Packets; when application data is included within the collection of packets, the DQ Frame represents a single complete logical unit of encapsulated application data.
- **DQ Control and Data Payload Packet Segment** Refers to the middle segment within the DQWA Transmission Sequence. This segment can carry both control and payload information within it.
- **DQ Segment** Refers to one of three logically distinct delineations within a DQ Transmission Sequence (listed as follows):
 - Access Request Sequence Segment:
 - DQ Control and Payload Packet Segment;
 - Feedback Packet Segment.
- **DQ Service Set (DQSS)** Refers to a set of nodes within a DQ Network that share a common peer-to-peer communication medium and are managed by a single authority that utilizes queues to control access to the DQ Network.
- **DQ Transmission Sequence** Refers the complete sequence of the three DQ Segments (i.e. ARS, Payload, Feedback) repeatedly, consistently, and always occurring in every DQWA transmission.
- **Feedback Window** Refers to the period of time within the DQ Transmission Sequence in which the Access Point or Cluster Head provides feedback to the nodes within the DQSS.

Queue Transmission Window – Refers to the period of time within the DQ Transmission Sequence in which the node at the top of the Transmission Queue is afforded the opportunity to transmit.

[0082] 4.0 Introduction to Distributed Queuing

Distributed Queuing as defined within this document describes a Layer 2 Protocol and PHY Transmission scheme that is agnostic to the underlying carrier. The initial and primary technology medium reaping the largest benefit from this technology is in the wireless realm; although there is no reason that it could not be equally applicable in a wire line based medium as well. The initial targeted benefit is as a Wireless Mobile Backhaul solution as well as a potential alternative to the entire series of wireless 802 based technologies, with specific attention to 802.11; while still being able to maintain coexistence with one of the very technology targets it is designed to replace.

[0083] Coexistence is not automatic; an implementer of DQ would have to design their product with coexistence explicitly set out as a goal. Essentially, some portion of the time would be spent processing DQ frames and the remainder of the time would be spent processing the 802.11 (or whatever other MAC it was replacing) for the remainder of the time.

[0084] The packet and frame formats have been specifically designed to take advantage of the relative collision free environment in the data content portion of the packet segment. Thus, there are two basic types of record keeping header formats:

- Those that are sent during every transmission sequence, otherwise known as packet segments.
- Those that are sent only for an entire frame, which can and often does span multiple packet segments.

[0085] The DQ Frame Header contains information normally found within an 802.11 type frame, but with one additional address in the event forwarding is necessary by either an address within the Distributed Queuing Service Set (DQSS) or to the greater network cloud beyond the Cluster Head.

The address types are listed below:

- Immediate DestinationDQ Network Address;
- Immediate SourceDQ Network Address;
- Cluster HeadDQ MAC Address;
- Actual Destination DQ MAC Address;
- · Original Source DQ MAC Address.

[0086] Only the first three addresses are required within normal DQ Frames; with the latter two addresses only necessary whenever forwarding is required beyond the current Distributed Queue Service Set (DQSS). A DQ Transmission Sequence, is depicted in Figure 1.

[0087] The DQ Transmission Sequence is divided into three separate segments (not counting the interval spacing):

- 1) the DQSS Access Request Sequence (ARS) Segment (also known as the "ARS Contention Window);
- 2) the DQ Control & Payload Segment (also known as the Queue Transmission Window);

¹Coexistence is not automatic; an implementer of DQ would have to design their product with coexistence explicitly set out as a goal. Essentially, some portion of the time would be spent processing DQ frames and the remainder of the time would be spent processing the 802.11 (or whatever other MAC it was replacing) for the remainder of the time.

3) and, the DQSS Feedback Packet Segment (also known as the Feedback Window).

[0088] Below is a brief overview of each segment:

- DQSS ARS Segment This segment, which is actually divided into three (3) subsegments, enables nodes within the DQSS with the ability to request permission for exchanging data with other nodes, including the Cluster Head.
- DQ Control& Payload Segment This segment represents both the addressing of the affected nodes exchanging data as well as the actual data itself. DQ Management Commands, Replies, and Requests are also communicated within this segment.
- DQSS Feedback Packet Segment This segment provides feedback representing DQSS Management & Record Keeping that is almost always in direct response to information contained in the immediate prior two (2) segments. It also has the intended side-effect of serving as a beacon, as it is transmitted at the end of every frame and should be used for synchronization purposes.

[0089] Up to five different nodes can successfully participate within a single transmission sequence; three within the ARS Segment with one per mini-slot, a fourth one within the DQ Control & Payload Segment, and finally a fifth from the Cluster Head within the Feedback Packet segment. Figure 2 depicts an example of a successful Transmission Sequence with five disparate transmitters.

[0090] The Protocol, MAC, and other operational aspects will now be explained in more detail.

[0091] 5.0 Distributed Queuing Operational Methodology

Like, the Basic Service Set in 802.11, DQ has a similar methodology in that a DQ Service Set can be viewed as a set of nodes within a network that communicate with each other while sharing a common distributed network that is managed by a central controlling authority, either an Access Point or a Cluster Head.

NOTE: Because DQ is by definition a distributed architecture, communication is therefore peer-to-peer even though "control" is centralized. What this means in practice is that the Cluster Head dictates which nodes have access to the queue; but all communication within the network is peer-to-peer.

[0092] 5.1 DQ Service Set Modes

A key component of the DQ Service Set concept is network security and the rules by which nodes may become members of a specific DQ Service Set.A DQSS can operate in one of three operational modes listed below the operational modes listed in decreasing order of centralized membership control:

- · Static Association Mode;
- Semi-Manual Association Mode;
- Promiscuous Mode;

[0093] Each of the modes will now be individually discussed in detail.

[0094] 5.1.1 DQSS Static Association Mode

In Static Association Mode, the DQ Service Set is completely pre-configured. New nodes may not request to join and can only become part of the DQSS either by directly adding nodes to an existing DQSS Configuration Database or by installing a completely new DQSS Configuration Database containing the desired nodes.

[0095] In response to the fact that a DQSS configured in Static Association Mode cannot add nodes in real time (doing so only through configuration); any attempt to submit a DQSS Membership Request Code Word during the ARS segment will be ignored.

[0096] 5.1.2 D QSS Semi-Manual Association Mode

A DQSS configured to be in Semi-Manual Association Mode has all of the capabilities of a Static Association Mode DQSS as well as the additional ability to add nodes in real time. There are two methods for which a node may acquire inclusion within a DQSS configured in DQ Semi-Manual Association Mode.

[0097] The first method for acceptance for a given node into a DQSS while in DQSS Semi-Manual Association Mode is via manual configuration as part of a DQSS Configuration Database. The second method utilizes a two-step process for any node outside of the current DQSS membership and described below:

- 1) First, the Candidate Node must issue a request for DQSS Inclusion.
- 2) Second, an external confirmation of the request from either an operator or configuration robot utility must explicitly accept the Candidate Node into the DQSS; presumably based upon some criteria established for admission. It is the latter act that serves as the basis for the moniker, "DQSS Semi-Manual Association Mode" since confirmation of inclusion requires an explicit action from an external source; presumably an operator or configuration robot utility.

[0098] 5.1.3 DQSS Promiscuous Association Mode

A DQSS configured to be in Promiscuous Association Mode has two methods for DQSS membership inclusion. As with all modes, the first method for inclusion into a DQSS is through configuration.

[0099] The second method for inclusion into an existing DQSS is similar to the second inclusion method listed for DQSS Semi-Manual Association Mode; however, no operator intervention is required except for the case of an operator explicitly desiring to exclude a node from the DQSS.

[0100] Thus, the only time operator intervention occurs during a DQSS operating in Promiscuous Association Mode is when an operator wishes to explicitly "blacklist" a candidate node; adding it to either a permanent blacklist or a blacklist that can be aged out.

[0101] An example of a situation in which permanent blacklisting may be desired would be if a paid subscriber within a physical locality like an Internet Café was delinquent in paying their subscriber fees and/or

had exceeded their usage. The subscriber could then be explicitly blacklisted until they brought their account current again and/or purchases additional time.

Presumably an operator or configuration robot utility

[0102] An example of temporary blacklisting could occur as a result of a background task monitoring network usage. If there was a limit as to the daily network activity for a particular subscriber and that subscriber had exceeded their limit, the Candidate Node of the subscriber could be placed on a blacklist that expired whenever their "lease" renewed again.

[0103] While there are certainly other, potentially more cogent examples, each of the above examples sufficiently illustrates the viability of the blacklist exclusion capability.

[0104] 5.2 DQSS Encryption Modes

Encryption may be used in any mode and can be implemented such that there is little, if any affect, as to how each Association Mode operates. There are two different types of encryption used within DQWA:

- o Encrypted Private Key Mode.
- o Encrypted Public Key Mode.

Both of these encryption methodologies will now be discussed in relation to their effects on operating modes.

[0105] 5.2.1 DQSS Encrypted Private (Shared) Key Mode

A DQSS configured to be in Encrypted Private Key Mode utilizes a symmetric encryption methodology with respect to both encrypting outgoing messages and decrypting incoming messages. Because both sides know what the decryption algorithm is, both sides may transmit the entire message encrypted, including the header.

[0106] The clear implication with this mode is that the encryption/decryption algorithms must be done within the PHY in hardware in order for the three operating modes (Static, Semi-Manual, and Promiscuous) to operate oblivious to the effects of encryption performed on the encapsulated data.

[0107] 5.2.2 DQSS Encrypted Public Key Mode

A DQSS configured to be in Encrypted Public Key Mode utilizes an asymmetric encryption methodology with respect to the encryption of outgoing messages and decrypting incoming messages.

[0108] Specifically, the shared (i.e. private) key is used for decrypting messages, but the public key must be utilized for encrypting messages. In this way, the entire message may be encrypted (as is done with Private (Shared) Key Mode), but the public key must be known in order to encrypt an outgoing message.

[0109] Thus, nodes wishing to "join" the network, regardless of the configuration must "listen" to the Feedback Packet in order to get the Public Key before they can transmit. The cogent point here is that although the public key is broadcast, it is done so in encrypted form using the "Private" key; thus adding an additional layer of security to this process.

[0110] 5.3 Dynamic Clustering

DQ supports Dynamic Clustering for the Control Point of DQNetwork Topology. If Dynamic Clustering is disabled, the Cluster Head serves as the static control point. Thus, if the Access Point goes down, so does the DQ Network. However, if Dynamic Clustering is enabled, the Dynamic Cluster Head Designation Order will be included within the DQSS and updated separately on a periodic basis.

[0111] There are multiple events that may trigger a Cluster Head Transition including traffic loading, hardware and/or power failures, energy consumption fairness criteria, or simply user discretion are a few of the more prominent events. Therefore, in order to support the various types of event triggers, there are multiple selections for the type of Cluster Topology configuration. The different Cluster Topology configuration types are listed below:

- Clustering Disabled The network is complete static, with one and only one node designated as
 the Access Point. Thus, if the Access Point fails, then so does the network connectivity.
- Clustering Enabled for Backup Only So long as the network is operating normally, the network is completely static; with a single node designated as the Access Point. However, in the event the designated Access Point fails, a succession of backup Access Points has been previously identified within the DQSS Table and thus assume the role of the Access Point according to their priority order and online status (i.e. the node that is both "online" and has the highest designated priority status becomes the Access Point if the current Access Point fails; if the highest designated priority status node is not online then the duty falls to the next lower designated priority status node). In the event there are no nodes that are online and have been designated as a backup Access Point, the network connectivity fails.
- Limited Clustering Enabled Normal Clustering is enabled for the network with this setting; however, only a limited set of designated nodes may participate as Cluster Heads.
- Clustering Enabled Normal Clustering is enabled for the network, with all nodes eligible for Cluster Head designation.

[0112] As alluded to above, for clustering to occur within a DQSS not only must the overall Cluster Topology be specified, but so must the Clustering Methodology.

[0113] 5.3.1 Clustering Methodologies

At present there are three distinct Clustering Methodologies:

- 1. Static Clustering;
- 2. Traffic Flow Clustering; and,
- 3. Traffic Flow with Topology Coverage Clustering.

[0114] More Clustering Methodologies may be added over time; but these three represent the initial set. Each of the three Clustering Methodologies will now be discussed.

[0115] 5.3.1.1 Static Clustering

Regardless of the setting of the Cluster Topology for a given DQSS, if the Cluster Methodology is set to "Static Clustering", then Dynamic Cluster is completely disabled. This is the only setting allowed for the "Clustering Disabled" and "Clustering Enabled for Backup Only" Cluster Topologies. If this setting is used for either the "Limited Clustering Enabled" or "Clustering Enabled" topologies, then the net effect is to force the overall network topology into that of "Clustering Enabled for Backup Only".

[0116] 5.3.1.2 Traffic Flow Clustering

Traffic Flow Clustering enables the Cluster Head to be located at the node providing the most efficiency with respect to being a "gate keeper" of the traffic flow. Because all communication and control is distributed and is not routed through a central spoke in order to communicate with other nodes within the DQSS, the only real advantage to the Cluster Head moving as the flow moves would be if the gateway can move with it. Meaning, the Cluster Head nodes have dual functionality with one port servicing the DQSS and other ports servicing one or more gateways.

[0117] 5.3.1.3 Traffic Flow with Topology Coverage Clustering

Traffic Flow with Topology Coverage Clustering enables the Cluster Head to be located at the node providing the greatest coverage for the current traffic flow. The distinction between this mode and standard "Traffic Flow Clustering" is that the former does not take into account the overall range of coverage of the client nodes within the DQSS.

[0118] Similar to standard "Traffic Flow Clustering", because all communication and control is distributed and is not routed through a central spoke in order to communicate with other nodes within the DQSS, the only real advantage to the Cluster Head moving as the flow moves would be if the gateway can move with it. Thus, as above, in order for this mode to be effective, Cluster Head nodes must have dual functionality with one port servicing the DQSS and other ports servicing one or more gateways.

[0119] 5.4 Additional DQ Service Set Rules

The Access Point or Cluster Head distributes the DQ Service Set on a periodic basis. No node may communicate with another node unless both nodes are contained within the same service set. Because of the strict adherence to this policy, in order for a node to join and subsequently communicate with other nodes, including the Cluster Head, within the DQSS, the following sequence of events must occur:

- a) The Access Point or Cluster Head must explicitly acknowledge and admit a node for inclusion into the DQSS:
- b) The Access Point or Cluster Head must then add it to the DQSS and perform either a complete or partial DQSS update of the DQSS Table to the nodes within the DQSS.

[0120] When possible, the Cluster Head will update the DQSS Table through update distributions as a means of saving time and bandwidth. There are few instances in which a complete DQSS distribution will occur, with the nominal occurrence being during initialization and start-up of the DQSS.

[0121] In short, the Cluster Head must first admit the node in the network and then secondarily inform the other nodes in the DQSS of the joining node's admission into the DQSS. The format of the DQSS Table is defined in section 9.1 on the "Distribute DQ Service Set Table (0x01)" command and includes the following:

- DQSS Configuration Data; providing information specifying the functional and operational makeup of the DQSS. Information included would be the DQSS Mode (i.e. Static, Manual, Promiscuous, Promiscuous-Shared Key), Encryption Indication, DQ Gateway Information, Maximum DQ Frame and DQ Packet Sizes,
- 48-Bit MAC Address of every Node within the DQSS.
- 12-Bit DQSS Address; this address is assigned by the Cluster Head to the individual nodes within the DQSS as a means of reducing the amount of overhead within the transmission stream.

²When possible, the Cluster Head will update the DQSS Table through update distributions as a means of saving time and bandwidth. There are few instances in which a complete DQSS distribution will occur, with the nominal occurrence being during initialization and start-up of the DQSS.

- 20-bit Code Word, assigned by the Cluster Head, and used for Access Requests to the Transmission Queue. This value is coupled with the DQSS Address on all access requests.
- Active or Inactive Indicators for Every DQ Member Given that the primary purpose of the DQSS
 Table is to maintain the integrity of the network, a DQSS Table should be viewed as an Object
 Oriented Encapsulation of a specific DQ Network.

[0122] 6.0 The Access Request Sequence

The purpose of the Access Request Sequence (ARS) is twofold:

- 1. To afford current members of the DQSS with an opportunity to request communication privileges with one or more of the other nodes (including the Cluster Head) within the network.
- 2. To simultaneously mitigate the potential for MAC & Data Payload collisions and hence, dropped frames resulting from corruption.

[0123] The latter is achieved by limiting the contention for access to the channel to a finite and predictable period of time. With the exception of the Cluster Head, all nodes must utilize this mechanism in order to access the MAC & Data Payload segment of the DQ Transmission Sequence.

[0124] 6.1 ARS Mechanics

The ARS Segment is divided into three (3) sub-parts, termed, Mini-Slots (MS) (as shown in Figure 3). This number was initially chosen based upon research[1] (i.e.Xu & Campbell, 1992) showing that the collision resolution process can be made to work faster than the data transmission process when the number of MS is

restricted to three (3). Increasing the number of MS beyond three (3) may introduce additional delay as well as adding increased overhead to the overall protocol resulting from the added delay.

[0125] The collision resolution process referenced above utilizes unique patterns transmitted by each soliciting device and a summation of those patterns in the event of a collision as a means for detecting collisions.

[0126] The operation of DQWA is based on the m-ternary feedback information on the state of each of the mini-slots. The Cluster Head must be able to distinguish between the three states:

- · Idle.
- · Success,
- · Collision,

for each mini-slot; as this information is crucial for the application of the protocol rules at the end of each frame. Adopting a patented technology [2] (i.e. Campbell & Xu, 2001) each node is assigned a unique bit pattern that has the property that when two or more ARS collide, the pattern of the overlapping signal is distinguishable from the original pattern of any single ARS; hence, the Cluster Head can detect the collision.

[0127] The preferred example patterns referenced in the paper are binomial coefficients; however, DQWA uses an increased hamming weight of four (4) in order to support a significantly increased number of unique code words than can otherwise be supported with a constant hamming weight of two (2). For instance, within a 32-bit word, there exists only 496-Code Words with a Hamming Weight of two; as compared to 35,960 Code Words having a Hamming Weight of four within the same 32-bits (almost two orders of magnitude more).

[0128] Given that DQWA is targeting potential MESH networks much larger than 496 nodes, larger Hamming Weights are necessitated for real-world implementation with (as mentioned above) four (4) being the current selected Hamming Weight.

[0129] Each node accepted into the network is assigned both a 12-bit Node Address and a 20-bit Code Word with a Hamming Weight of four (4) (as shown in Figure 4).

[0130] When a collision does occur, it is a relatively straightforward process to determine since the Hamming Weight will be greater than four (4). There are 4,845 4-Bit Code Words within a 20-bit binary string; thus, the worst case probability that a collision could occur and result in a valid Code Word is less than ½ of a percent (0.46%). However, since the Code Word is also coupled with the Node Address, there is an additional safeguard procedure to ensure that any anomalous undetected collision is immediately detected.

[0131] The aforementioned ternary decision can be subsequently determined as follows:

- Idle (i.e. no signal in ARS Mini-Slot) Received Signal is below the RSSI (Noise) Threshold.
- Success A demodulation resulting in a precise hamming weight of four (4) and a correlated (i.e. correct) code word value and node address combination.

 Collision – Any signal detected above the noise (RSSI) threshold not resulting in a translation into the digital domain of a code word with a hamming weight of four (4) and/or not having a correlated (i.e. correct) code word value and node address combination.

[0132] The Cluster Head will respond with the collision results as part of the DQSS Management Segment in order to clarify any potential ambiguities.

[0134] 6.2 ARS QoS Support

It is presumed that in most cases, DQWA will be utilized with some level of QoS enabled; if so, two additional fields are added to the ARS Mini-Slot structure so that the feedback packet can adequately determine the queuing order for each node:

- · Requested Message Payload Limit, and
- Requested Message Priority;

[0135] Each field is 4-bits, which in turn expands each ARS Mini-Slot to a Preamble plus 40-bits of information. Figure 5 depicts the expanded ARS Segment with QoS support. Figure 6 depicts the expanded version of an individual Mini-Slot.

[0136] The contents of each field will now be detailed; although a more complete explanation can be found in section 10 on "The DQSS Management Segment (Feedback Packet (FP))."

[0137] 6.2.1 QoS Requested Message Payload Limit

Table 1 specifies each setting and corresponding reservation amount:

QoS Requested Message Payload Setting	QoS Message Payload Value
(in binary)	(in bytes)
0000	4,096
0001	8,192
0010	12,288
0011	16,384
0100	20,480
0101	24,576
0110	28,672
0111	32,768
1000	36,864
1001	40,960
1010	45,056
1011	49,152
1100	53,248
1101	57,344
1110	61440
1111	65,536

Table 1 - ARS QoS Requested Message Payload Limit Settings

[0138] The implied value specified by the QoS Requested Message Payload setting is used by the Cluster Head to determine the relative placement in the distribution queue of the requesting station.

[0139] 6.2.2 QoS Requested Message Priority

The values used for the QoS Requested Message Priority field are the same values used within a frame, as detailed in section 8.1.1.1.9 on "Quality of Service (QoS) Level –111b."

[0140] There are eight priority levels, thus only three bits are required, leaving the uppermost bit unused and reserved (as shown in Figure 7). The priority levels increase linearly, thus a priority level of '0' is of the lowest priority and a priority level of '7' is of the highest priority. DQWA does not define what the individual priority levels mean, leaving that up to the network layer protocols sitting on top of DQWA.

[0141] 6.3 DQSS Node Addressing within the ARS

DQSS Network addresses are 12-bits in length, however, only the lower 10-bits are assignable for the dynamic portion of a valid address; as the upper two bits have special meaning. Both bits along with the rest of the DQSS Network Address are shown in Figure 8:

[0142] The DQSS Node Addressing will now be explained within the context of the ARS; addition detail of the DQSS Node Address field is found in subsequent sections.

[0143] 6.3.1 DQSS Node Address Field

6.3.1.1 DQSS Node Cluster Bit

NOTE: This bit is NOT used within the ARS; but will be explained here since this bit is part of the DQSS Node Address Field. This bit should ALWAYS be zero during the ARS; as the Cluster Head may preempt the Transmit Queue any time it deems necessary to do so and is not restricted to the transmit request process as the rest of the nodes within the DQSS are.

[0144] The MSB of the address is reserved for the Cluster Head. This is particularly helpful if the Network Topology moves and the Cluster Head moves with it. Thus, allowing any node to maintain its original identity both before and after assuming the duties of the Cluster Head. In this way, the DQSS table maintains consistency regardless of which node is currently in charge of the network.

[0145] 6.3.1.2 DQSS Node Join Request Bit

The next most significant bit (bit 1) is used by nodes wishing to join the network. In order for an unknown node to be considered for admittance to the DQSS, it must satisfy two conditions:

- 1) The "Join Request" Bit shown in **Error! Reference source not found.** must be set within the DQSS Node Address Field.
- 2) The "DQSS Mini-Cluster" Sub-Field must set '7' (i.e. "111b").

[0146] The "DQSS Individual Address" Sub-Field may be any value between '0' and "127" (i.e. a span of 128-values). The complete list of predefined Hamming Weights and DQSS Network Addresses may be found in Appendix A.

[0147] 6.3.1.3 DQSS MiniCluster SubField

These three bits are used to allow the network administrator to organize nodes in accordance to their own internal policies. Assignable values are between '0' ("000b") and '6' ("110b"), with '7' ("111b") reserved for "Join Requests" and "Broadcasts".

[0148] 6.3.1.4 DQSS Individual Address SubField

These seven bits are used for assigning individual addresses, with any value between '0' and "126" assignable for an individual DQSS Network Address. The only time "127" may be used during the ARS is during a "Join Request." As "127" is otherwise set aside for "Directed Broadcasts" and regular "Broadcasts" for all Mini-Cluster Sub-Field values except for '7' (i.e. "111b").

[0149] 6.4 ARS Join Requests

As outlined in the prior section, "Join Requests" may choose between any one of 128 values for the DQSS Individual Address Sub-Field and any one of 17-values for the Code Word. So long as predefined values are selected for those fields as well as the "Join Request" bit being set; the Join Request will be considered valid.

[0150] 7.0 DQ Message

A DQ Message is what is presented as the interface between the MAC and Network layers and consists of the below fields:

- 1) Address Fields;
- 2) Frame Length Field;
- 3) Data Payload area;
- 4) and a Frame Check Sequence (FCS) Field.

[0151] Figure 9 depicts a complete DQ Frame:

Each of the above four logical divisions of the DQ Frame Structure will now be detailed.

[0152] 7.1 DQ Frame Address Fields

The DQ Frame has two variants for addressing:

- Internal DQSS Network Addresses;
- External DQ MAC Address.

[0153] A DQSS Network address is a 12-bit address that uniquely identifies the DQ Node within a specific DQSS Network and was explained in detail in section 6.3 and depicted in **Error! Reference source not found.**

[0154] A DQ Network Address is at most 12-bits, with the uppermost 4-bits of each DQ Network Address set aside and reserved for future expansion. Thus, the maximum number of nodes potentially supported within a given DQSS is 4,096; minus selected addresses set aside for explicit functionalities. However, as explained in sections 6.3.1.1 and 6.3.1.2, the uppermost two bits have special significance; thus preventing them from being used as normal address bits. Meaning, the number of stations that can actually be delineated is 210 (i.e. 1,024).

[0155] The DQ MAC Address adheres to standard IEEE 802 MAC-48/EUI-48 formatting and structure with the intent it eventually be adopted into the overall 802 standard.

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[0156] 7.1.1 The Standard Addressing DQ Frame Header

With few exceptions (Application Data intermediate frames being noted as the most common exception) most DQ Frames include the DQ Network Address of both the destination and sender along with the DQ MAC Address of the DQ Cluster Head/Access Point. This is known as the "Standard Addressing DQ Frame Header" and is shown in Figure 10.

[0157] The Standard DQ Address Header contains the three Address Fields:

- 1) The Immediate Destination DQ Network Address;
- 2) The Immediate Source DQ Network Address;
- 3) The Cluster Head DQ MAC Address

with With the first two addresses being internal DQ Network Addresses and the Cluster Head being a standard DQ MAC Address.

[0158] 7.1.2 The Extended Addressing DQ Frame Header

The Extended Addressing DQ Frame Header extends the Standard Addressing DQ Frame Header by adding the DQ MAC Addresses of the original sender and final destination nodes (as shown in Figure 11). This frame is only required if the Final Destination and Original Source Nodes are not part of the same DQSS. In this case, the "Destination DQ Network Address" is set to that of the Access Point or Cluster Head.

[0159] Therefore, with one exception, any time the Access Point or Cluster Head is specified as the "Destination DQ Network Address", the Extended Address DQ Frame Header is used. The lone exception is whenever the Access Point or Cluster Head is also the final destination; in which case only the Standard DQ Frame Header is utilized.

4-With the exception being that the Access Point or Cluster Head is the Final Destination Node.

[0160] 7.2 DQ Frame Payload Length Field

As the name implies, the length contained here specifies the number of bytes within the frame payload and must be a number between 256 and 4,096 bytes. Meaning, 256-bytes is the minimum size Frame Payload and 4,096-bytes is the maximum size Frame Payload.

[0161] 7.3 DQ Payload Field

This field carries the data payload of the frame. Other than length, there are no restrictions to the contents of this field. If there are not sufficient bytes to fill the minimum size DQ Payload field, the missing bytes will be zero filled.

[0162] 7.4 DQ Frame Check Sequence (FCS) Field

The FCS is a 32-Bit CRC located immediately following the last byte transmitted for a given frame and covers the entire frame contents, including the four bytes of the FCS.

[0163] 8<u>.0</u> DQ Data & Control Window

The DQ Data & Control Window is the portion of the Transmission Sequence in which application data is communicated and is the most complex of the three segments comprising the Transmission Sequence. The three segments are: The DQSS ARS Segment, the DQ Control & Payload Segment, and the DQSS Feedback Packet Segment.

[0164] All DQ Packet Segments are comprised of:

- 1) A DQ Packet Segment Pre-Header;
- 2) An optional Management Information Sub-Header and Directives;
- 3) An optional Frame Data Payload section;
- 4) A 4-Byte Packet Check Sequence (PCS).

NOTE: Although both (2) and (3) above are optional, all DQ Packet Segments must contain one or both of them.

[0165] The most basic DQ Packet is one in which the entire frame is contained within the packet and has no MI Directives. However, DQ Packet Segments may also contain Management Information Directives, Frame Check Sequence (if the entire frame is not contained within one Packet Segment), and may even exclude a Data Payload portion altogether if only MI Directives are required for a given Packet Segment.

[0166] The individual elements of the above Basic DQ Packet Segment will now be detailed in order to provide the framework for the more complex Packet Segments discussed later in this section.

[0167] 8.1 The Basic DQ Packet Segment with No MI Directive

The Basic DQ Packet is shown in Figure 12. The Basic DQ Packet Segment may be between 278 and 4,134 bytes in length and is comprised (at a minimum) of the DQ Packet Segment Pre-header, the DQ Frame Header, the DQ Frame Data Payload, and the Packet Check Sequence (PCS); but also may include a Frame Length Field and Frame Check Sequence (FCS) depending upon the type of packet, (as discussed throughout this section).

[0168] 8.1.1 The DQ Packet Segment PreHeader

Figure 13 depicts the physical layout of the DQ MAC Basic Pre-Header. All DQ Packets have a DQ Packet Segment Pre-Header and have the following three fields as listed below:

- The Packet Segment Control Field,
- · The Packet Segment Length Field, and
- The Sequence Control Field.

These three fields provide the majority of the information required for describing the Packet Segment's content. An illustration of the Pre-Header is provided below:

s-The three segments are: The DQSS ARS Segment, the DQ Control & Payload Segment, and the DQSS Feedback Packet Segment.

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[0169] The first field, the Packet Segment Control field, provides detailed information about both the packet itself as well as the current configuration of the network. This is most helpful to nodes listening in that may need to adjust their own configuration prior to attempting to enter into the DQSS. The settings within the Packet Segment Control field detail the contents of the packet, including whether or not the DQ Frame portion of the packet is an entire frame or one in a series of fragmented frame segments.

[0170] The remaining next two fields, the Packet Segment Length and Sequence Control fields will now be detailed.

[0171] 8.1.1.1 Packet Segment Control Field

The contents of the Packet Segment Control bits determine the size and content of the rest of the frame and therefore are the most interesting portion of this segment. The fields and meanings are shown in Figure 14.

[0172] 8.1.1.1.1 DQ Protocol Version

The DQ Protocol Version is initially set to "0000b" and is set aside as a backwards compatibility measure in anticipation that future use of DQ will expand beyond what is currently envisioned and hence require structure and format changes.

[0173] 8.1.1.1.2 Data Fragment Management

The Data Fragment Management field provides information to the recipient node enabling the receiving station to discern if this frame is part of a larger fragmented frame or not. If so, these settings directly determine whether or not the packet contains a Frame Length field as is the case with completely encapsulated frames, the initial segment of a fragmented frame, and the initial segment of a fragmented resumed frame. Additionally, the settings contained within determine if the DQ Packet contains Application Data and/or if the packet simply contains DQSS Management Information. The settings and associated meanings are provided in Table 2.

	Bits			
4	5	6	Description	
0	0	0	Management Packet with no Application Data	
0	0	1	First Data Packet of Frame	
0	1	0	First Resumed Data Packet of Frame	
0	1	1	Resumed Frame with Final Data Packet of Frame	
1	0	0	Final Data Packet of Frame	
1	0	1	Intermediate Data Packet of Frame	
1	1	0	Complete Frame within Data Packet	
1	1	1	Reserved	

Table 2 - Data Fragment Management Field Settings

[0174] 8.1.1.1.2.1 Management Frame - 000b

This field indicates that there is no Application Data within this packet. Therefore, the packet is strictly for management and control purposes.

[0175] 8.1.1.1.2.2 First Data Packet of Frame - 001b

This value indicates the frame is fragmented and that the packet is the initial packet in a sequence of packets comprising the overall frame. All necessary address fields for the frame are included with this packet as well as a frame length field.

[0176] Figure 15 depicts the header part of this frame, including the DQ Packet Segment Pre-Header. NOTE: There is no FCS within this packet since the FCS does not occur until the final Packet representing the Frame.

[0177] 8.1.1.1.2.3 First Resumed Data Packet of Frame – 010b

This value indicates the frame transmission sequence was previously preempted by higher priority traffic and that the packet is the first packet in the resumption of the frame transmission sequence; but is NOT the last packet within the sequence. There is a separate delineation for an occurrence of the latter (see section 8.1.1.1.2.4 below).

[0178] All necessary address fields for the frame are repeated within this packet including the frame length field with one minor exception, the length contained with the frame length field specifies the number of bytes left within the resumed frame including the bytes within the current packet.

The DQ Packet Segment Pre-Header and the Resumed DQ Fragmented Frame Header showing all of the DQ Frame fields repeated are shown in Figure 16. NOTE: The above figure is an example of a Standard Addressing DQ Frame.

•An Extended Addressing DQ Frame would have additional addresses (as detailed in section 7.1.2, "The Extended Addressing DQ Frame Header")

[0179] 8.1.1.1.2.4 Resumed Frame with Final Data Packet of Frame – 011b

This value indicates the frame is fragmented and that this is the first packet following a pause in the packet sequence transmissions for that frame, as the transmission sequence was previously preempted by a higher priority form of traffic. It also indicates that this is the final fragment within the sequence.

[0180] The Frame Address fields are again repeated for this final packet; however, the frame length field is not included since it is superfluous given that the DQ Packet Segment Pre-Header contains the length of the entire packet and hence the payload length can be easily calculated from it.

[0181] Figure 17 depicts the DQ Packet Segment Pre-Header and DQ Frame header of a Resumed Frame that occurs as the Final Data Packet of the Frame: NOTE: The figure is an example of a Standard Addressing DQ Frame. An Extended Addressing DQ Frame would have additional addresses, as detailed in section 7.1.2, "The Extended Addressing DQ Frame Header".

[0182] Another consequence of a multi-packet frames is that in addition to an Packet Control Sequence (PCS) validating the contents of the overall packet; there is a Frame Check Sequence, validating the contents of the overall frame.

[0183] Figure 18 depicts the complete structure of this type of packet, including the FCS and PCS. NOTE: The figure is an example of a Standard Addressing DQ Frame. <u>An Extended Addressing DQ Frame would have additional addresses</u>, as detailed in section 7.1.2, "The Extended Addressing DQ Frame Header".

[0184] 8.1.1.1.2.5 Last Data Packet of Frame – 100b

This value indicates that the data segment contains the last segment of a larger message. There are no Frame Address fields following the DQ Packet Segment Pre-Header for this case; but there is an FCS as well as PCS (see Error! Reference source not found. Error! Reference source not found).

[0185] Figure 19 depicts the complete structure of this type of packet, including the FCS and PCS. NOTE: There are NO address fields within this packet.

[0186] 8.1.1.1.2.6 Intermediate Data Packet of Frame – 110b

This value indicates that the data segment contains an intermediate segment of a larger message. There are noFrame Address fields following the DQ Packet Segment Pre-Header for this case; nor is there an FCS.

[0187] Figure 20 depicts the complete packet of this type of packet, including the FCS and PCS. NOTE: There are NO address fields within this packet.

[0188] 8.1.1.1.2.7 Complete Frame within Data Packet – 011b

This value indicates that the DQ Packet contains the entire DQ Frame. The Frame address fields immediately follow the DQ Packet Segment Pre-Header; however, there is neither a Frame Length field nor a Frame Check Sequence (FCS) field, as both would be redundant if included.

[0189] Figure 21 depicts the complete structure of this type of packet, including the FCS and PCS. NOTE: Figure 21 is an example of a Standard Addressing DQ Frame. <u>An Extended Addressing DQ Frame would have additional addresses</u>, as detailed in section 7.1.2, "The Extended Addressing DQ Frame Header".

[0190] 8.1.1.1.2.8 Reserved -111b

This field is reserved for future use.

[0191] 8.1.1.1.3 Management Directive (MD) Bit (Bit 7)

If set, this bit indicates that there is Management Information (MI) Header within the packet and that the MI Sub-Header is located immediately following the DQ Packet Segment Pre-Header and before the Address and/or Payload fields if any.

[0192] 8.1.1.1.4 Retransmission Bit (Bit 8), RB

If set, this bit indicates that the packet is a retransmission of a previously transmitted packet. This can be used by the receiver station to determine that this may be a duplicate transmission of prior frames as result of an Acknowledgement being lost.

[0193] 8.1.1.1.5 Dynamic Clustering Enable Bit, DC

If set, this bit indicates that the Cluster Head is Dynamic; thus the Cluster Head will change in real time according to predefined rules.

[0194] 8.1.1.1.6 Power Management Bit, PM

If set, this bit indicates the Power Management mode that the station will be in after the transmission of the frame; this bit is used by stations that are changing state from Power Save to Active or vice-versa.

[0195] 8.1.1.1.7 Encryption Bit, EE

This bit indicates encryption is enabled.

[0196] 8.1.1.1.8 Priority Queuing Enable Bit, PQ

If set, this bit indicates priority queuing is enabled

[0197] 8.1.1.1.9 Quality of Service (QoS) Level -111b

This field only has meaning if the Priority Queuing Enable Bit is set and there is Application Data within the payload; otherwise these bits are unused. There are eight levels of priority, with the level of priority increasing linearly with the value of the QoS bits:

Lowest Priority: "000b"
Highest Priority: "111b"

[0198] 8.1.1.2 DQ Frame Length Field

The Frame Length field provides the length of the entire DQ Frame, including the FCS.

[0199] 8.1.1.3 DQ Sequence Control Fields

The Sequence Control Fields keep maintain control of the application data exchanged between two DQSS nodes.

[0200] 8.1.1.3.1 DQ Sequence Number Field

The Sequence Number identifies the last packet the sending station sent to the destination station. The Sequence Number is checked at the receiver for missing or duplicated packet. A station receiving numbered information packet advances its Nr count if the packet received is in sequence and does not have errors. The

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receiving station's Nr count will be equal to the Ns in the next expected information packet or one greater than the Ns in the last packet received. The receiver confirms accepted numbered information packet by returning its Nr count to the transmitting station.

[0201] If the incoming Ns does not agree with the receiving station's Nr count, the packet is out of sequence and Nr does not advance. The Nr in the out-of-sequence packet is still valid for confirming transmitted packets.

[0202] The count range for Ns and Nr is 256, using the digits 0 through 255. Once the sequence number 255 is reached, the count wraps back around to 0. The Nr and Ns counts are initialized to 0.

[0203] 8.1.1.3.2 DQ Acknowledgment Number Field

The Acknowledgement Number identifies the last packet the sending station has received from the destination station.

[0204] The Acknowledgment Number is checked at the destination for missing or duplicated packets. If the incoming Nr does not agree with the receiving stations Ns, the receiving station must reset its Ns to match the incoming Nr and resend any missing packets not received by the sending station the next time it gains control of the queue.

[0205] The count range for Ns and Nr is 256, using the digits 0 through 255. Once the sequence number 255 is reached, the count wraps back around to 0. The Nr and Ns counts are initialized to 0.

[0206] 8.1.2 Frame Address Fields

DQ Packets utilize the same addresses as do DQ Frames; however, because DQ Packets can and often are much smaller; these frames are NOT repeated for multi-packet frames unless otherwise explicitly noted (such as in the case of a "resumed" frame packet sequence).

[0207] 8.1.3 Frame Length Field

As mentioned in section 4, and other sections 8, 8.1.1, and subsections within 8.1.1.1.2, a DQ Frame can be encapsulated either within one single DQ Packet (as detailed in section 8.1.1.1.2.7 above) or divided across multiple packets.

[0208] If the frame is to be divided across multiple packets, it will always contain a length field prior to the data payload area within the initial packet of the frame sequence and will also contain a Frame Check Sequence following the data payload area within the last packet of the frame sequence. Otherwise, if the entire frame is encapsulated within a single DQ Packet, neither of these fields is required since both can be deduced from similar fields within the DQ Packet structure (i.e. the Packet Length Field in lieu of the Frame Length Field and Packet Check Sequence in lieu of the Frame Check Sequence).

[0209] 8.1.4 Packet Data Payload < Describe Data Payload area here>

This segment contains the actual data or body data that is the intended communication.

₹See Sections 4, 8, 8.1.1, and several subsections within 8.1.1.1.2.

[0210] 8.1.5 Frame Check Sequence (FCS)

The FCS is a 32-Bit CRC located immediately following the last byte transmitted for a given frame. The only time the FCS is included within an actual DQ Packet is immediately following the last packet of a multi-packet Frame sequence (see **Error! Reference source not found.** for an example).

[0211] 8.1.6 Packet Check Sequence (PCS)

The PCS is a 32-Bit CRC located immediately following the last byte transmitted for a given packet and occurs in every single packet. The structure of a typical packet and PCS is shown in Figure 22. NOTE: The PCS is applied to the entire packet plus the four bytes of the PCS.

[0212] 8.2 The Basic DQ Packet Segment with MI Directive

The basic DQ Packet with an MI Directive area is shown in Figure 23. The basic DQ Packet is between 276 and 4,130 bytes in length and is comprised of the DQ Packet Segment Pre-header, the DQ Frame Header, the DQ Management Information Sub-Header and Associated MI Payload (if any), the DQ Frame Data Payload, and the Packet Check Sequence (PCS).

[0213] 8.2.1 The Management Information (MI) Directive SubHeader

The MI Sub-Header provides a mechanism for Communication and Control Directives and associated data between DQSS Nodes and has only one mandatory field, the DQSS Management Information Directive Field (as shown in Figure 24).

[0214] Any additional fields within the MI Sub-Header are MI Directive dependent. The below list details the current list and associated values of all the DQSS MI Directives:

0x00: Reserved

0x01: Distribute DQ Service Set Table Command (no acknowledgement. See details in Section 8.2.2.1)

0x02: Mandatory Disconnect Command (no acknowledgement)

0x03: Disconnect Request (from Station to Cluster Head)

0x04: Disconnect Confirmed Response(from Cluster Head to Station)

0x05: Join Request (from Station to Cluster Head)

0x06: Join Accepted Response(from Cluster Head to Station)

0x07: Re-cluster Command (from NEW Cluster Head)

0x08: Re-cluster Acknowledge Response(from each individual station within cluster)

0x09: Link Quality SNR Exchange Request (from Cluster Head to Station)

0x0A: Link Quality SNR Exchange Response (from Station to Cluster Head)

0x0B: Bandwidth Management Command (from Cluster Head to Station)

0x0C: Bandwidth Management Acknowledge Response (from Station to Cluster Head)

0x0D: Maximum Frame Size Command (no acknowledgement) (from Cluster Head to Stations)

0x0E: Switch Queue Command (no response)

0x0F: Pause Queue Command (no response)

0x10: Pause Queue, Enable Join Request for Mini-Slot 1

0x11: Pause Queue, Enable Join Request for Mini-Slot 2

0x12: Pause Queue, Enable Join Request for Mini-Slot 3

0x13: Resume Queue Command

[0215] However, while the above list enumerates all of the possible Directives; those directives are divided between ones that are can be transmitted during the Feedback Packet segment and those that can be transmitted during the DQ Packet Segment.

[0216] 8.2.2 Management Information (MI) Directive used within DQ Packet Segment

The Directives discussed within this section can only occur within the DQ Packet Segment.

[0217] 8.2.2.1 Distribute DQ Service Set Table (0x01)

This command is a minimum of bytes in length and can only be sent by the Access Point/Cluster. <u>Figure 25</u> depicts the global parameter area of the Distribute DQSS Table Command. NOTE: all Bits labeled as 'R' are unused and hence reserved. The DQ Service Set Table is divided into two sets of parameters:

- 1) The first set of parameters are applicable to the entire table and shown below:
 - a. The Security Status of the DQSS:
 - i. No Encryption (1-Byte);
 - ii. Public Key Encryption (1-Byte);
 - iii. Private (Shared) Key Encryption (1-Byte).
 - b. Public Encryption Key (16-Bytes: this field only exists when Security Status is set to "Public Key Encryption"; otherwise, this field is not part of the DQSS Table).
 - c. Maximum Packet Payload Limitation of the DQSS (1-Byte).
 - d. Number of Configured DQSS Nodes (2-Bytes).

Figure 25 depicts the global parameter area of the Distribute DQSS Table Command.

NOTE: all Bits labeled as 'R' are unused and hence reserved.

- 2) The remaining parameters are applicable for all DQSS Nodes with one entry per Node within the DQSS including the Access Point or Cluster Head:
 - DQSS MAC Address.
 - Assigned DQSS Network Address.
 - · Assigned DQSS Hamming Weight.
 - Assigned Cluster Head Priority.
 - Assigned QoS Node Priority. This field should be zero (0) for most networks and should only be used if there are specific nodes that need higher priority than others nodes. In those cases in which QoS is on and two nodes are in the queue with the same QoS priority traffic waiting to be sent, the one with the higher priority (if any) moves to the top of the queue for that specific priority setting. NOTE: This only effects traffic of equivalent QoS priorities. It does NOT affect higher priority traffic from a lower priority node. Higher priority traffic is always serviced before lower priority traffic regardless of the priority of the node.

- Assigned Bandwidth Status:
 - o No Bandwidth Guarantee;
 - o Limited/Restricted bandwidth;
 - o Guaranteed bandwidth.
- Assigned Bandwidth Setting of each station (i.e. limit or minimum guaranteed value) when applicable.

[0218] 8.2.2.1.1 DQSS Security Status & Public Encryption Key Fields

In order to provide the maximum degree of security within the network, the encryption switch is found within the first byte following the DQSS Table Command byte. Only the least significant lower two bits are valid. The remaining upper six bits are unused and hence reserved.

[0219] 8.2.2.1.1.1 DQSS No Encryption ("00b")

Whenever the Security Status field is set to No Encryption, then there are no additional fields; thus the first two bytes of DQSS table are simply the command and security status fields as shown in Figure 26. In this case, the remaining bytes within the DQSS Table are encrypted using the Shared Encrypted Key possessed by all of the DQSS member stations.

[0220] 8.2.2.1.1.2 DQSS Public KeyEncryption ("01b")

Whenever the Security Status field is set to Public Key Encryption, then the immediate subsequent field is the Public Key field as shown in Figure 27. In this case, the remaining bytes within the DQSS Table are encrypted using the Public Key.

[0221] 8.2.2.1.1.3 DQSS Shared KeyEncryption ("10b")

Whenever the Security Status field is set to Shared Key Encryption, then there is no public key field. The DQSS Table Command and Security Status fields are shown in Figure 28. In this case, the remaining bytes within the DQSS Table are encrypted using the Shared Encrypted Key possessed by all of the DQSS member stations.

[0222] 8.2.2.2 Maximum Payload

The Maximum Payload field enables specifies the maximum number of bytes allowed within the payload portion of a DQSS Information Frame. The minimum allowed payload is 256-bytes and the maximum allowed payload is 4,096-bytes.

[0223] Only the lower four bits of this field are used with the remaining upper four bits being reserved. All payload specifications are given in 256-byte increments with "0000b" representing 256-bytes and "1111b" representing 4,096-bytes.

[0224] 8.2.2.3 Number of Configured DQSS Nodes

This field can never be zero, since the Access Point or Cluster Head always counts as part of the network. Hence, zero a setting of "00000000b" is considered invalid.

[0225] 8.2.2.4 DQSS Table Entries per Node

The remaining fields within the DQSS Table are on a per node basis and in the following order for each entry:

- Bytes: 0-5 DQSS MAC Address.
- Bytes: 6-9:
 - ☐ Assigned DQSS Hamming Weight.
 - ☐ Assigned DQSS Network Address.
- Bytes: 10-11 Assigned Cluster Head Priority.
- Byte: 12 Assigned QoS Node Priority.
- Byte: 13 Assigned Bandwidth Status:
 - o No Bandwidth Guarantee;
 - o Limited/Restricted bandwidth;
 - o Guaranteed bandwidth.
- Bytes: 14-15 Assigned Bandwidth Setting of each station.

[0226] Figure 29 depicts a Single Table Record within the Distribute DQSS Table Command.

[0227] 8.2.2.5 Mandatory Disconnect Command

This command is 5-bytes in length and can only be sent by the Cluster Head to a DQSS Client Node. It cannot be ignored by the DQSS Client Node. The format of the Mandatory Disconnect is shown in Figure 30.

[0228] No response is expected or desired from the affected DQ Client Node. If the DQ Client Node attempts any further communication other than a request to "Join the DQSS", the Cluster Head will in turn respond with another MD command.

- Distribute DQ Service Set Table --
- 0x14: Mandatory Disconnect (no acknowledgement)
- 0x15: Disconnect Request (from Station to Cluster Head)
- 0x16: Disconnect Confirmed (from Cluster Head to Station)
- 0x17: Join Request (from Station to Cluster Head)
- 0x18: Join Accepted (from Cluster Head to Station)
- 0x19: Re-cluster Command (from NEW Cluster Head)
- 0x20: Re-cluster Acknowledge (from each individual station within cluster)
- 0x21: Link Quality SNR Exchange Request (from Cluster Head to Station)
- 0x0G: Link Quality SNR Exchange Response (from Station to Cluster Head)
- 0x0H: Bandwidth Management Command (from Cluster Head to Station)
- Ox0I: Bandwidth Management Acknowledge (from Station to Cluster Head)
- 0x0J: Maximum Frame Size Command (no acknowledgement) (from Cluster Head to Stations)
- 0x0K: Switch Queue
- 0x0L: Pause Queue
- 0x22: Pause Queue, Enable Join Request for Mini-Slot 1
- 0x23: Pause Queue, Enable Join Request for Mini-Slot 2
- 0x24: Pause Queue, Enable Join Request for Mini-Slot 3

0x25: Resume Queue [LAZ1]

[0229] The MI Sub-Header provides a mechanism for Communication and Control Directives and associated data between DQSS Nodes and has only one mandatory field, the DQSS.

[0228] 8.3 Frame Control Sequence (FCS)

The MCS is a 32-Bit CRC located immediately following the last byte transmitted for a given message. This field is not part of a frame whose payload comprises a complete message. There are only two instances where this field would appear:

- When the Data Fragment Management field is set to "011b" Indicating the frame is a "Resumed Message with Final Data Segment" frame. Meaning, it is the last frame of previously interrupted sequence of frames for the associated message.
- When the Data Fragment Management field is set to "100b" Indicating the frame is a "Final Data Segment" frame. Meaning, it is the last frame of sequence of frames for the associated message.

[0229] In these two instances, the format of the MAC & Data Payload Segment are shown in Figure 31. NOTE: The MCS is only applied to the payload portion of the message plus the four bytes of the MCS.

[0230] 9.0 Management Information (MI) Directives

The MI Directives are used to maintain and control the network. Directives initiated by the Access Point or Cluster Head are usually intended to maintain the order and integrity of the overall DQSS network. While directives initiated by DQSS Client Nodes are generally used for a specific service or action for that particular DQSS Client Node. Each MI Directive will now be individually detailed, including a complete description of its use, its structure, and intended actions resulting whenever it is used.

- 9.1 Distribute DQ Service Set Table (0x01)
- 9.2 Mandatory Disconnect (0x02)
- 9.3 Disconnect Request (0x03)
- 9.4 Disconnect Confirmed (0x04)
- 9.5 DQSS Join Request (0x05)
- 9.6 DQSS Join Confirmed (0x06)
- 9.7 Re-Cluster Command (0x07)
- 9.8 Re-Cluster Acknowledge (0x08)
- 9.9 Link Quality SNR Exchange Request (0x09)
- 9.10 Link Quality SNR Exchange Response (0x0A)
- 9.11 Bandwidth Management Command (0x0B)
- 9.12 Bandwidth Management Acknowledge (0x0C)
- 9.13 Maximum Frame Size Command (0x0D)
- 9.14 Maximum Frame Size Command (0x0E)
- 9.15 Switch Queue Command (0x0F)
- 9.16 Pause Queue Command (0x10)

[0231] This command can only occur within the Feedback Packet and causes the immediate cessation of application data for all subsequent transmission sequences pending further notice. This includes the case of the command being issued during the transmission of a multi-frame message. 8

[0232] ⁸If the command occurs within the sequence of a multi-frame message; the continuation of that message is paused effectively immediately and is not resumed until a "Resume Queue" command is later issued by the Cluster Head.

[0233] 9.17 Pause Queue, Enable Join Request for ARS MiniSlot One (1) Command (0x11)

This command has the same effect as the Pause Queue Command (0x10), but with two additional side-effects:

- 1) The ARS is eliminated during the immediate transmission sequence; thus this is the notification to all stations so that they may abide by it.
- 2) The Station making the join request within ARS Mini-Slot One (1) of the prior ARS segment is directed to issue a Join Request Directive within the DQ Control & Data Payload Segment of the next transmission sequence.

[0234] Assuming successful transmission of this directive, the subsequent feedback packet will contain feedback as to the determination and resultant actions of the Join Request for ARS Mini-Slot One (1).

[0235] 9.18 Pause Queue, Enable Join Request for ARS Mini-Slot Two (2) Command (0x12) This command has the same effect as the Pause Queue Command (0x10), but with two additional side-effects:

- 1) The ARS is eliminated during the immediate transmission sequence; thus this is the notification to all stations so that they may abide by it.
- 2) The Station making the prior join request within ARS Mini-Slot Two (2) of the prior ARS segment is directed to issue a Join Request Directive within the DQ Control & Data Payload Segment of the next transmission sequence.

[0236] Assuming successful transmission of this directive, the subsequent feedback packet will contain feedback as to the determination and resultant actions of the Join Request for ARS Mini-Slot Two (2).

[0237] 9.19 Pause Queue, Enable Join Request for ARS Mini-Slot Three (3) Command (0x13) This command has the same effect as the Pause Queue Command (0x10), but with two additional side-effects:

- 1) The ARS is eliminated during the immediate transmission sequence; thus this is the notification to all stations so that they may abide by it.
- 2) The Station making the prior join request within ARS Mini-Slot Three (3) of the prior ARS segment is directed to issue a Join Request Directive within the DQ Control & Data Payload Segment of the next transmission sequence.

[0238] Assuming successful transmission of this directive, the subsequent feedback packet will contain feedback as to the determination and resultant actions of the Join Request for ARS Mini-Slot Three (3).

[0239] 9.20 Resume Queue Command (0x0E)

10.0 The DQSS Management Segment (Feedback Packet (FP)) The DQSS Management Segment has three primary functions:

- 1) To provide the Cluster Head a means in which to manage the DQSS and associated nodes from the perspective of membership, Quality of Service (QoS), and both queues (i.e. Data Queue and Request Queue).
- 2) To provide feedback to the other nodes in the system for both data and control information.
- 3) To signify and thus mark the end of a single transmission sequence, therefore providing a beacon to all stations for synchronizations purposes.

[0240] Figure 32 represents the structure of the FP and fulfills the above three requirements.

As shown above, the DQSS Management Segment or FP consists of five sections:

- Preamble
- ARS Response
- MI Command or Response
- Sequence Control
- Feedback Packet 8-Bit CRC.

Other than the "Preamble," which is self-explanatory; each one will now be described in detail.

[0241] 10.1 ARS Response

Similar to the actual ARS, which has three Mini-Slots, the response to the ARS contains a one-to-one correlation as shown in Figure 33. With the precise contents for each ARS Mini-Slot Response divided into three separate sections as shown in Figure 34.

10.2 FP MI Command/Response

10.3 Sequence Control

10.4 Feedback Packet CRC

[0242] 11.0 Technology Roadmap

This is dated and will be updated after I finish the Feedback Packet Segment (JBS - 10/28/2011).

[0243] 11.1 Basic Distributed Queuing Wireless Arbiter (DQWA) – Wireless LAN Implementation This would be for a basic proof of concept.

Features:

- Static Access Point
- Fixed Sub-stations
- No Hidden Nodes

Target: Replacement for Wi-Fi

[0244] 11.2 Full DQWA – Wireless LAN Implementation

Introduce mobility with the client stations, which by default also adds in hidden nodes.

Features:

- Static Access Point
- · Fixed or Mobile Client Stations
- Hidden Nodes
- Relay Feature for Hidden Nodes, with 2-hop limit for relay

Target: Replacement for Wi-Fi

[0245] 11.3 Full Distributed Queuing Wireless Arbiter (DQWA) with QoS – Wireless LAN Implementation

Features:

- Static Access Point
- Fixed or Mobile Client Stations
- Hidden Nodes
- Relay Feature for Hidden Nodes, with 2-hop limit for relay
- Priority Queuing for supporting QoS

Target: Replacement for Wi-Fi

[0246] 11.4 Basic Distributed Queuing Wireless Arbiter (DQWA) with QoS and Guaranteed Bandwidth – Wireless LAN Implementation

Features:

- Static Access Point
- Fixed or Mobile Client Stations
- Hidden Nodes
- Relay Feature for Hidden Nodes, with 2-hop limit for relay
- Priority Queuing for supporting QoS
- · Guaranteed Bandwidth

Target: Replacement for Wi-Fi

[0247] 11.5 Distributed Queuing Mac protocol for Adhoc Networks (DQMAN) – Wireless LAN Implementation

Features

- StaticAccess Point or Dynamic Cluster Head (i.e. ad-hoc clustering)
- Fixed or Mobile Client Stations
- Hidden Nodes
- Relay Feature for Hidden Nodes, with 2-hop limit for relay

Target: Replacement for Wi-Fi.

[0248] 11.6 Distributed Queuing Mac protocol for Adhoc Networks (DQMAN) with QoS – Wireless LAN Implementation

Features

- Static Access Point or Dynamic Cluster Head (i.e. ad-hoc clustering)
- Fixed or Mobile Client Stations
- Hidden Nodes
- Relay Feature for Hidden Nodes, with 2-hop limit for relay
- Priority Queuing for supporting QoS

Target: Replacement for Wi-Fi.

[0249] 11.7 Distributed Queuing Mac protocol for Adhoc Networks (DQMAN) with QoS and Guaranteed Bandwidth – Wireless LAN Implementation

Features

- Static Access Point or Dynamic Cluster Head (i.e. ad-hoc clustering)
- Fixed or Mobile Client Stations
- · Hidden Nodes
- Relay Feature for Hidden Nodes, with 2-hop limit for relay
- Priority Queuing for supporting QoS
- · Guaranteed Bandwidth

Target: Replacement for Wi-Fi.

[0250] 11.8 Full DQWA with Routing Support with QoS and Guaranteed Bandwidth – Wireless Corporation Area Network (CAN) Implementation

(Introduce Routing Connectivity between DQWA Wireless LANs).

Features:

- Static CAN Base Station
- Fixed CAN Router Sub-stations
- No Hidden CAN Nodes
- Routing Support of QoS
- · Routing Support of Guaranteed Bandwidth

Target: Replacement for Fiber or Copper based Ethernet Corporate Backbone.

Two additional comments here:

- 1) Trying to route Ad-Hoc Networks would be very difficult without a centralized conduit; so having the Router Sub-Stations be fixed seems to be the logical choice in this instance.
- 2) Assuming the Router Sub-Station is fixed; then it could be part of a Static Access Point, providing of course the RF issues can be worked out because of the dual antennas. The dual functionality would be very similar to a DSL Wireless Router within people's homes.

Appendix A. Predefined Network Addresses and Code Words used for Joining DQSS

When requesting to join the network; a requesting node must transmit that request during the ARS by using a combination of a predefined set of Network Addresses and Code Words as well as enabling the "Join" bit.

A.1 Predefined

Network Addresses used for Join Requests

The below list enumerate the 128-different DQ Network Addresses that can be used when requesting to join a DQSS network (NOTE: these values cover both the Mini-Cluster and Individual Address Sub-Fields within the DQSS Network Address):

• 0x0380 (896)	• 0x03C1 (961)	• 0x03DD (989)	• 0x03F9 (1017)
• 0x0381 (897)	• 0x03C2 (962)	• 0x03DE (990)	• 0x03FA (1018)
• 0x0382 (898)	• 0x03C3 (963)	• 0x03DF (991)	• 0x03FB (1019)
• 0x0383 (899)	• 0x03C4 (964)	• 0x03E0 (992)	• 0x03FC (1020)
• 0x0384 (900)	• 0x03C5 (965)	• 0x03E1 (993)	• 0x03FD (1021)
• 0x0385 (901)	• 0x03C6 (966)	• 0x03E2 (994)	• 0x03FE (1022)
• 0x0386 (902)	• 0x03C7 (967)	• 0x03E3 (995)	• 0x03FF (1023)
• 0x0387 (903)	• 0x03C8 (968)	• 0x03E4 (996)	
• 0x0388 (904)	• 0x03C9 (969)	• 0x03E5 (997)	
• 0x0389 (905)	• 0x03CA (970)	• 0x03E6 (998)	
• 0x038A (906)	• 0x03CB (971)	• 0x03E7 (999)	
• 0x038B (907)	• 0x03CC (972)	• 0x03E8 (1000)	
• 0x038C (908)	• 0x03CD (973)	• 0x03E9 (1001)	
• 0x038D (909)	• 0x03CE (974)	• 0x03EA (1002)	
• 0x038E (910)	• 0x03CF (975)	• 0x03EB (1003)	
• 0x038F (911)	• 0x03D0 (976)	• 0x03EC (1004)	
• 0x0390 (912)	• 0x03D1 (977)	• 0x03ED (1005)	
• 0x0391 (913)	• 0x03D2 (978)	• 0x03EE (1006)	
• 0x0392 (914)	• 0x03D3 (979)	• 0x03EF (1007)	
• 0x0393 (915)	• 0x03D4 (980)	• 0x03F0 (1008)	
• 0x0394 (916)	• 0x03D5 (981)	• 0x03F1 (1009)	
• 0x0395 (917)	• 0x03D6 (982)	• 0x03F2 (1010)	
• 0x0396 (918)	• 0x03D7 (983)	• 0x03F3 (1011)	
• 0x0397 (919)	• 0x03D8 (984)	• 0x03F4 (1012)	
• 0x0398 (920)	• 0x03D9 (985)	• 0x03F5 (1013)	
• 0x0399 (921)	• 0x03DA (986)	• 0x03F6 (1014)	
• 0x039A (922)	• 0x03DB (987)	• 0x03F7 (1015)	

• 0x039B (923) • 0x03DC (988) • 0x03F8 (1016)

A.2 Predefined Code Words used for Join Requests

The below list represents 17-different Code Words that can be used when requesting to join a DQSS network:

• 0000000000000001111	• 00000001111000000000
• 0000000000000011110	• 00000011110000000000
• 0000000000000111100	• 00000111100000000000
• 0000000000001111000	• 00001111000000000000
• 0000000000011110000	• 000111100000000000000
• 0000000000111100000	• 0011110000000000000000
• 0000000001111000000	• 0111100000000000000000000000000000000
• 0000000011110000000	• 1111000000000000000000000000000000000
• 0000000111100000000	

NOTE: Even if the "Join Bit" within the requesting ARS Mini-Slot is set, but either the Code Word and/or the Network Address are NOT from these lists, the request will be ignored.

Appendix B. List of Allowed 20Bit Code Words with Hamming Weight of 4

There are a total of 4,845 Code Words with a Hamming Weight of 4 in a 20-bit string. With the exception of those shown in **BOLD RED** (which are reserved and not usable as a regular DQ Node Network Address), the below list represents all of the aforementioned 20-Bit Code Words with a Hamming Weight of 4:

0x0000F ==> 000000000000001111	0x20094 ==> 0010000000010010100
0x00017 ==> 000000000000010111	0x20098 ==> 0010000000010011000
0x0001B ==> 00000000000011011	0x200A1 ==> 0010000000010100001
0x0001D ==> 000000000000011101	0x200A2 ==> 0010000000010100010
0x0001E ==> 000000000000011110	0x200A4 ==> 0010000000010100100
0x00027 ==> 000000000000100111	0x200A8 ==> 0010000000010101000
0x0002B ==> 000000000000101011	0x200B0 ==> 0010000000010110000
0x0002D ==> 000000000000101101	0x200C1 ==> 0010000000011000001
0x0002E ==> 000000000000101110	0x200C2 ==> 0010000000011000010
0x00033 ==> 000000000000110011	0x200C4 ==> 0010000000011000100
0x00035 ==> 000000000000110101	0x200C8 ==> 0010000000011001000
0x00036 ==> 000000000000110110	0x200D0 ==> 0010000000011010000
0x00039 ==> 000000000000111001	0x200E0 ==> 0010000000011100000
0x0003A ==> 000000000000111010	0x20103 ==> 0010000000100000011
0x0003C ==> 000000000000111100	0x20105 ==> 0010000000100000101
0x00047 ==> 000000000001000111	0x20106 ==> 0010000000100000110
0x0004B ==> 000000000001001011	0x20109 ==> 0010000000100001001
0x0004D ==> 000000000001001101	0x2010A ==> 0010000000100001010
0x0004E ==> 000000000001001110	0x2010C ==> 0010000000100001100
0x00053 ==> 000000000001010011	0x20111 ==> 0010000000100010001
0x00055 ==> 000000000001010101	0x20112 ==> 0010000000100010010
0x00056 ==> 000000000001010110	0x20114 ==> 0010000000100010100
0x00059 ==> 000000000001011001	0x20118 ==> 0010000000100011000
0x0005A ==> 000000000001011010	0x20121 ==> 0010000000100100001
0x0005C ==> 000000000001011100	0x20122 ==> 0010000000100100010
0x00063 ==> 000000000001100011	0x20124 ==> 0010000000100100100
0x00065 ==> 000000000001100101	0x20128 ==> 0010000000100101000
0x00066 ==> 000000000001100110	0x20130 ==> 0010000000100110000
0x00069 ==> 000000000001101001	0x20141 ==> 0010000000101000001
0x0006A ==> 000000000001101010	0x20142 ==> 0010000000101000010

0x20144 ==> 0010000000101000100
0x20148 ==> 0010000000101001000
0x20150 ==> 0010000000101010000
0x20160 ==> 0010000000101100000
0x20181 ==> 0010000000110000001
0x20182 ==> 0010000000110000010
0x20184 ==> 0010000000110000100
0x20188 ==> 0010000000110001000
0x20190 ==> 0010000000110010000
0x201A0 ==> 0010000000110100000
0x201C0 ==> 0010000000111000000
0x20203 ==> 0010000001000000011
0x20205 ==> 0010000001000000101
0x20206 ==> 0010000001000000110
0x20209 ==> 0010000001000001001
0x2020A ==> 0010000001000001010
0x2020C ==> 0010000001000001100
0x20211 ==> 0010000001000010001
0x20212 ==> 0010000001000010010
0x20214 ==> 0010000001000010100
0x20218 ==> 0010000001000011000
0x20221 ==> 0010000001000100001
0x20222 ==> 0010000001000100010
0x20224 ==> 0010000001000100100
0x20228 ==> 0010000001000101000
0x20230 ==> 0010000001000110000
0x20241 ==> 0010000001001000001
0x20242 ==> 0010000001001000010
0x20244 ==> 0010000001001000100
0x20248 ==> 0010000001001001000
0x20250 ==> 0010000001001010000
0x20260 ==> 0010000001001100000
0x20281 ==> 0010000001010000001
0x20282 ==> 0010000001010000010
0x20284 ==> 0010000001010000100
0x20288 ==> 0010000001010001000

0x000E2 ==> 0000000000011100010	0x20290 ==> 0010000001010010000
0x000E4 ==> 0000000000011100100	0x202A0 ==> 0010000001010100000
0x000E8 ==> 0000000000011101000	0x202C0 ==> 0010000001011000000
0x000F0 ==> 0000000000011110000	0x20301 ==> 00100000001100000001
0x00107 ==> 0000000000100000111	0x20302 ==> 0010000001100000010
0x0010B ==> 0000000000100001011	0x20304 ==> 00100000001100000100
0x0010D ==> 0000000000100001101	0x20308 ==> 0010000001100001000
0x0010E ==> 0000000000100001110	0x20310 ==> 0010000001100010000
0x00113 ==> 0000000000100010011	0x20320 ==> 0010000001100100000
0x00115 ==> 0000000000100010101	0x20340 ==> 0010000001101000000
0x00116 ==> 00000000001001110	0x20380 ==> 00100000001110000000
0x00119 ==> 0000000000100011001	0x20403 ==> 00100000010000000011
0x0011A ==> 0000000000100011010	0x20405 ==> 00100000010000000101
0x0011C ==> 0000000000100011100	0x20406 ==> 00100000010000000110
0x00123 ==> 0000000000100100011	0x20409 ==> 00100000010000001001
0x00125 ==> 0000000000100100101	0x2040A ==> 00100000010000001010
0x00126 ==> 0000000000100100110	0x2040C ==> 00100000010000001100
0x00129 ==> 0000000000100101001	0x20411 ==> 00100000010000010001
0x0012A ==> 0000000000100101010	0x20412 ==> 00100000010000010010
0x0012C ==> 0000000000100101100	0x20414 ==> 00100000010000010100
0x00131 ==> 0000000000100110001	
0x00132 ==> 0000000000100110010	0x20418 ==> 00100000010000011000
0x00134 ==> 0000000000100110100	0x20421 ==> 00100000010000100001
0x00138 ==> 0000000000100111000	0x20422 ==> 00100000010000100010
0x00143 ==> 0000000000101000011	0x20424 ==> 00100000010000100100
0x00145 ==> 0000000000101000101	0x20428 ==> 00100000010000101000
0x00146 ==> 0000000000101000110	0x20430 ==> 00100000010000110000
0x00149 ==> 0000000000101001001	0x20441 ==> 00100000010001000001
0x0014A ==> 0000000000101001010	0x20442 ==> 00100000010001000010
0x0014C ==> 0000000000101001100	0x20444 ==> 00100000010001000100
0x00151 ==> 0000000000101010001	0x20448 ==> 00100000010001001000
0x00152 ==> 0000000000101010010	0x20450 ==> 00100000010001010000
0x00154 ==> 0000000000101010100	0x20460 ==> 00100000010001100000
0x00158 ==> 000000000010111000	0x20481 ==> 00100000010010000001
0x00161 ==> 0000000000101100001	0x20482 ==> 00100000010010000010
0x00162 ==> 0000000000101100010	0x20484 ==> 0010000010010000100

0x00164 ==> 0000000000101100100	0x20488 ==> 0010000010010001000
0x00168 ==> 0000000000101101000	0x20490 ==> 0010000010010010000
0x00170 ==> 0000000000101110000	0x204A0 ==> 0010000010010100000
0x00183 ==> 0000000000110000011	0x204C0 ==> 0010000010011000000
0x00185 ==> 0000000000110000101	0x20501 ==> 0010000010100000001
0x00186 ==> 0000000000110000110	0x20502 ==> 0010000010100000010
0x00189 ==> 0000000000110001001	0x20504 ==> 0010000010100000100
0x0018A ==> 0000000000110001010	0x20508 ==> 0010000010100001000
0x0018C ==> 0000000000110001100	0x20510 ==> 0010000010100010000
0x00191 ==> 0000000000110010001	0x20520 ==> 0010000010100100000
0x00192 ==> 0000000000110010010	0x20540 ==> 0010000010101000000
0x00194 ==> 0000000000110010100	0x20580 ==> 0010000010110000000
0x00198 ==> 0000000000110011000	0x20601 ==> 00100000011000000001
0x001A1 ==> 0000000000110100001	0x20602 ==> 00100000011000000010
0x001A2 ==> 0000000000110100010	0x20604 ==> 00100000011000000100
0x001A4 ==> 0000000000110100100	0x20608 ==> 00100000011000001000
0x001A8 ==> 0000000000110101000	0x20610 ==> 00100000011000010000
0x001B0 ==> 0000000000110110000	0x20620 ==> 00100000011000100000
0x001C1 ==> 0000000000111000001	0x20640 ==> 0010000011001000000
0x001C2 ==> 0000000000111000010	0x20680 ==> 0010000011010000000
0x001C4 ==> 0000000000111000100	0x20700 ==> 00100000011100000000
0x001C8 ==> 0000000000111001000	0x20803 ==> 0010000010000000011
0x001D0 ==> 0000000000111010000	0x20805 ==> 0010000010000000101
0x001E0 ==> 0000000000111100000	0x20806 ==> 0010000010000000110
0x00207 ==> 0000000001000000111	0x20809 ==> 0010000010000001001
0x0020B ==> 0000000001000001011	0x2080A ==> 0010000010000001010
0x0020D ==> 0000000001000001101	0x2080C ==> 00100000100000001100
0x0020E ==> 0000000001000001110	0x20811 ==> 0010000010000010001
0x00213 ==> 000000000100011011	0x20812 ==> 0010000010000010010
0x00215 ==> 000000000100010101	0x20814 ==> 00100000100000010100
0x00216 ==> 000000000100010110	0x20818 ==> 00100000100000011000
0x00219 ==> 000000000100011001	0x20821 ==> 00100000100000100001
0x0021A ==> 0000000001000011010	0x20822 ==> 00100000100000100010
0x0021C ==> 0000000001000011100	0x20824 ==> 00100000100000100100
0x00223 ==> 0000000001000100011	0x20828 ==> 00100000100000101000
0x00225 ==> 000000000100100101	0x20830 ==> 00100000100000110000

0x00226 ==> 0000000001000100110	0x20841 ==> 00100000100001000001
0x00229 ==> 0000000001000101001	0x20842 ==> 00100000100001000010
0x0022A ==> 0000000001000101010	0x20844 ==> 00100000100001000100
0x0022C ==> 0000000001000101100	0x20848 ==> 00100000100001001000
0x00231 ==> 0000000001000110001	0x20850 ==> 00100000100001010000
0x00232 ==> 0000000001000110010	0x20860 ==> 00100000100001100000
0x00234 ==> 0000000001000110100	0x20881 ==> 00100000100010000001
0x00238 ==> 0000000001000111000	0x20882 ==> 00100000100010000010
0x00243 ==> 0000000001001000011	0x20884 ==> 00100000100010000100
0x00245 ==> 0000000001001000101	0x20888 ==> 00100000100010001000
0x00246 ==> 0000000001001000110	0x20890 ==> 00100000100010010000
0x00249 ==> 0000000001001001001	0x208A0 ==> 00100000100010100000
0x0024A ==> 0000000001001001010	0x208C0 ==> 00100000100011000000
0x0024C ==> 0000000001001001100	0x20901 ==> 00100000100100000001
0x00251 ==> 0000000001001010001	0x20902 ==> 00100000100100000010
0x00252 ==> 0000000001001010010	0x20904 ==> 00100000100100000100
0x00254 ==> 0000000001001010100	0x20908 ==> 00100000100100001000
0x00258 ==> 0000000001001011000	0x20910 ==> 00100000100100010000
0x00261 ==> 0000000001001100001	0x20920 ==> 00100000100100100000
0x00262 ==> 0000000001001100010	0x20940 ==> 00100000100101000000
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0x00268 ==> 0000000001001101000	0x20A01 ==> 00100000101000000001
0x00270 ==> 0000000001001110000	0x20A02 ==> 00100000101000000010
0x00283 ==> 0000000001010000011	0x20A04 ==> 00100000101000000100
0x00285 ==> 0000000001010000101	0x20A08 ==> 00100000101000001000
0x00286 ==> 0000000001010000110	0x20A10 ==> 00100000101000010000
0x00289 ==> 0000000001010001001	0x20A20 ==> 00100000101000100000
0x0028A ==> 0000000001010001010	0x20A40 ==> 00100000101001000000
0x0028C ==> 0000000001010001100	0x20A80 ==> 00100000101010000000
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0x00294 ==> 0000000001010010100	0x20C02 ==> 0010000011000000010
0x00298 ==> 0000000001010011000	0x20C04 ==> 0010000011000000100
0x002A1 ==> 0000000001010100001	0x20C08 ==> 00100000110000001000
0x002A2 ==> 0000000001010100010	0x20C10 ==> 00100000110000010000
0x002A4 ==> 0000000001010100100	0x20C20 ==> 00100000110000100000

0x002B0 ==> 0000000001010110000	0x20C80 ==> 00100000110010000000
0x002C1 ==> 0000000001011000001	0x20D00 ==> 00100000110100000000
0x002C2 ==> 0000000001011000010	0x20E00 ==> 00100000111000000000
0x002C4 ==> 0000000001011000100	0x21003 ==> 0010000100000000011
0x002C8 ==> 0000000001011001000	0x21005 ==> 0010000100000000101
0x002D0 ==> 0000000001011010000	0x21006 ==> 0010000100000000110
0x002E0 ==> 0000000001011100000	0x21009 ==> 0010000100000001001
0x00303 ==> 0000000001100000011	0x2100A ==> 0010000100000001010
0x00305 ==> 0000000001100000101	0x2100C ==> 0010000100000001100
0x00306 ==> 0000000001100000110	0x21011 ==> 0010000100000010001
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0x0030A ==> 0000000001100001010	0x21014 ==> 0010000100000010100
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0x00311 ==> 0000000001100010001	0x21021 ==> 0010000100000100001
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0x00314 ==> 0000000001100010100	0x21024 ==> 0010000100000100100
0x00318 ==> 0000000001100011000	0x21028 ==> 0010000100000101000
0x00321 ==> 0000000001100100001	0x21030 ==> 00100001000000110000
0x00322 ==> 0000000001100100010	0x21041 ==> 00100001000001000001
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0x00328 ==> 0000000001100101000	0x21044 ==> 0010000100001000100
0x00330 ==> 0000000001100110000	0x21048 ==> 0010000100001001000
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0x00344 ==> 0000000001101000100	0x21081 ==> 00100001000010000001
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0x00350 ==> 0000000001101010000	0x21084 ==> 00100001000010000100
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0x00381 ==> 0000000001110000001	0x21090 ==> 00100001000010010000
0x00382 ==> 0000000001110000010	0x210A0 ==> 00100001000010100000
0x00384 ==> 0000000001110000100	0x210C0 ==> 00100001000011000000
0x00388 ==> 0000000001110001000	0x21101 ==> 00100001000100000001
0x00390 ==> 0000000001110010000	0x21102 ==> 00100001000100000010
0x003A0 ==> 0000000001110100000	0x21104 ==> 0010000100010000100
0x003C0 ==> 0000000001111000000	0x21108 ==> 00100001000100001000

0x00407 ==> 000000001000000111	0x21110 ==> 00100001000100010000
0x0040B ==> 000000001000001011	0x21120 ==> 00100001000100100000
0x0040D ==> 000000001000001101	0x21140 ==> 00100001000101000000
0x0040E ==> 000000001000001110	0x21180 ==> 00100001000110000000
0x00413 ==> 000000001000011011	0x21201 ==> 00100001001000000001
0x00415 ==> 0000000010000010101	0x21202 ==> 00100001001000000010
0x00416 ==> 0000000010000010110	0x21204 ==> 00100001001000000100
0x00419 ==> 0000000010000011001	0x21208 ==> 00100001001000001000
0x0041A ==> 000000001000011010	0x21210 ==> 00100001001000010000
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0x00423 ==> 0000000010000100011	0x21240 ==> 00100001001001000000
0x00425 ==> 0000000010000100101	0x21280 ==> 00100001001010000000
0x00426 ==> 0000000010000100110	0x21300 ==> 00100001001100000000
0x00429 ==> 0000000010000101001	0x21401 ==> 00100001010000000001
0x0042A ==> 0000000010000101010	0x21402 ==> 0010000101000000010
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0x00431 ==> 0000000010000110001	0x21408 ==> 00100001010000001000
0x00432 ==> 0000000010000110010	0x21410 ==> 00100001010000010000
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0x0044C ==> 000000001001100	0x21804 ==> 0010000110000000100
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0x00462 ==> 0000000010001100010	0x21900 ==> 0010000110010000000
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0x00468 ==> 0000000010001101000	0x21C00 ==> 0010000111000000000
0x00470 ==> 0000000010001110000	0x22003 ==> 0010001000000000011
0x00483 ==> 0000000010010000011	0x22005 ==> 0010001000000000101

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0x00489 ==> 0000000010010001001	0x2200A ==> 0010001000000001010
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0x0048C ==> 0000000010010001100	0x22011 ==> 0010001000000010001
0x00491 ==> 0000000010010010001	0x22012 ==> 0010001000000010010
0x00492 ==> 0000000010010010010	0x22014 ==> 0010001000000010100
0x00494 ==> 0000000010010010100	0x22018 ==> 0010001000000011000
0x00498 ==> 0000000010010011000	0x22021 ==> 0010001000000100001
0x004A1 ==> 0000000010010100001	0x22022 ==> 0010001000000100010
0x004A2 ==> 0000000010010100010	0x22024 ==> 0010001000000100100
0x004A4 ==> 0000000010010100100	0x22028 ==> 0010001000000101000
0x004A8 ==> 0000000010010101000	0x22030 ==> 00100010000000110000
0x004B0 ==> 0000000010010110000	0x22041 ==> 0010001000001000001
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0x00505 ==> 0000000010100000101	0x22084 ==> 0010001000010000100
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0x00530 ==> 0000000010100110000	0x22201 ==> 00100010001000000001
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0x00542 ==> 0000000010101000010	0x22204 ==> 0010001000100000100
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0x00550 ==> 0000000010101010000	0x22220 ==> 00100010001000100000
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0x00581 ==> 0000000010110000001	0x22280 ==> 00100010001010000000
0x00582 ==> 0000000010110000010	0x22300 ==> 00100010001100000000
0x00584 ==> 0000000010110000100	0x22401 ==> 00100010010000000001
0x00588 ==> 0000000010110001000	0x22402 ==> 0010001001000000010
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0x005A0 ==> 0000000010110100000	0x22408 ==> 00100010010000001000
0x005C0 ==> 0000000010111000000	0x22410 ==> 00100010010000010000
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0x0060C ==> 0000000011000001100	0x22801 ==> 00100010100000000001
0x00611 ==> 0000000011000010001	0x22802 ==> 0010001010000000010
0x00612 ==> 0000000011000010010	0x22804 ==> 0010001010000000100
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0x00618 ==> 0000000011000011000	0x22810 ==> 00100010100000010000
0x00621 ==> 0000000011000100001	0x22820 ==> 00100010100000100000
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0x00624 ==> 0000000011000100100	0x22880 ==> 00100010100010000000
0x00628 ==> 0000000011000101000	0x22900 ==> 00100010100100000000
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0x00641 ==> 0000000011001000001	0x22C00 ==> 00100010110000000000
0x00642 ==> 0000000011001000010	0x23001 ==> 00100011000000000001
0x00644 ==> 0000000011001000100	0x23002 ==> 0010001100000000010
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0x00650 ==> 0000000011001010000	0x23008 ==> 0010001100000001000
0x00660 ==> 0000000011001100000	0x23010 ==> 00100011000000010000
0x00681 ==> 0000000011010000001	0x23020 ==> 00100011000000100000
0x00682 ==> 0000000011010000010	0x23040 ==> 00100011000001000000
0x00684 ==> 0000000011010000100	0x23080 ==> 00100011000010000000

0x00688 ==> 0000000011010001000	0x23100 ==> 0010001100010000000
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0x006A0 ==> 0000000011010100000	0x23400 ==> 0010001101000000000
0x006C0 ==> 0000000011011000000	0x23800 ==> 0010001110000000000
0x00701 ==> 00000000011100000001	0x24003 ==> 0010010000000000011
0x00702 ==> 0000000011100000010	0x24005 ==> 0010010000000000101
0x00704 ==> 00000000011100000100	0x24006 ==> 0010010000000000110
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0x00720 ==> 00000000011100100000	0x2400C ==> 0010010000000001100
0x00740 ==> 0000000011101000000	0x24011 ==> 0010010000000010001
0x00780 ==> 0000000011110000000	0x24012 ==> 0010010000000010010
0x00807 ==> 0000000010000000111	0x24014 ==> 0010010000000010100
0x0080B ==> 000000010000001011	0x24018 ==> 0010010000000011000
0x0080D ==> 000000010000001101	0x24021 ==> 0010010000000100001
0x0080E ==> 0000000010000001110	0x24022 ==> 0010010000000100010
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0x00815 ==> 00000000100000010101	0x24028 ==> 0010010000000101000
0x00816 ==> 000000010000010110	0x24030 ==> 0010010000000110000
0x00819 ==> 000000010000011001	0x24041 ==> 0010010000001000001
0x0081A ==> 000000010000011010	0x24042 ==> 0010010000001000010
0x0081C ==> 000000010000011100	0x24044 ==> 0010010000001000100
0x00823 ==> 0000000100001100011	0x24048 ==> 0010010000001001000
0x00825 ==> 000000010000100101	0x24050 ==> 0010010000001010000
0x00826 ==> 0000000100001101	0x24060 ==> 0010010000001100000
0x00829 ==> 0000000100000101001	0x24081 ==> 0010010000010000001
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0x0082C ==> 000000010000101100	0x24084 ==> 0010010000010000100
0x00831 ==> 0000000100000110001	0x24088 ==> 0010010000010001000
0x00832 ==> 0000000100000110010	0x24090 ==> 0010010000010010000
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0x00838 ==> 0000000100000111000	0x240C0 ==> 00100100000011000000
0x00843 ==> 0000000100001000011	0x24101 ==> 00100100000100000001
0x00845 ==> 000000010001000101	0x24102 ==> 00100100000100000010
0x00846 ==> 000000010001100	0x24104 ==> 00100100000100000100
0x00849 ==> 0000000100001001001	0x24108 ==> 0010010000100001000

0x0084A ==> 00000001000101010	0x24110 ==> 0010010000100010000
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0x00862 ==> 0000000100001100010	0x24208 ==> 0010010000100001000
0x00864 ==> 0000000100001100100	0x24210 ==> 00100100001000010000
0x00868 ==> 00000000100001101000	0x24220 ==> 00100100001000100000
0x00870 ==> 00000000100001110000	0x24240 ==> 00100100001001000000
0x00883 ==> 0000000100010000011	0x24280 ==> 00100100001010000000
0x00885 ==> 000000010001000101	0x24300 ==> 00100100001100000000
0x00886 ==> 000000010001000110	0x24401 ==> 00100100010000000001
0x00889 ==> 0000000100010001001	0x24402 ==> 0010010001000000010
0x0088A ==> 0000000100010001010	0x24404 ==> 0010010001000000100
0x0088C ==> 0000000100010001100	0x24408 ==> 00100100010000001000
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0x00892 ==> 00000000100010010010	0x24420 ==> 00100100010000100000
0x00894 ==> 0000000100010010100	0x24440 ==> 00100100010001000000
0x00898 ==> 0000000100010011000	0x24480 ==> 00100100010010000000
0x008A1 ==> 00000000100010100001	0x24500 ==> 00100100010100000000
0x008A2 ==> 00000000100010100010	0x24600 ==> 00100100011000000000
0x008A4 ==> 00000000100010100100	0x24801 ==> 00100100100000000001
0x008A8 ==> 00000000100010101000	0x24802 ==> 0010010010000000010
0x008B0 ==> 00000000100010110000	0x24804 ==> 0010010010000000100
0x008C1 ==> 0000000100011000001	0x24808 ==> 0010010010000001000
0x008C2 ==> 0000000100011000010	0x24810 ==> 0010010010000010000
0x008C4 ==> 0000000100011000100	0x24820 ==> 00100100100000100000
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0x008E0 ==> 0000000100011100000	0x24900 ==> 00100100100100000000
0x00903 ==> 0000000100100000011	0x24A00 ==> 00100100101000000000
0x00905 ==> 0000000100100000101	0x24C00 ==> 00100100110000000000
0x00906 ==> 0000000100100000110	0x25001 ==> 00100101000000000001
0x00909 ==> 0000000100100001001	0x25002 ==> 00100101000000000010

0x0090A ==> 0000000100100001010	0x25004 ==> 0010010100000000100
0x0090C ==> 0000000100100001100	0x25008 ==> 0010010100000001000
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0x00912 ==> 00000000100100010010	0x25020 ==> 00100101000000100000
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0x00918 ==> 00000000100100011000	0x25080 ==> 00100101000010000000
0x00921 ==> 00000000100100100001	0x25100 ==> 00100101000100000000
0x00922 ==> 0000000010010010010	0x25200 ==> 00100101001000000000
0x00924 ==> 00000000100100100100	0x25400 ==> 00100101010000000000
0x00928 ==> 00000000100100101000	0x25800 ==> 00100101100000000000
0x00930 ==> 00000000100100110000	0x26001 ==> 00100110000000000001
0x00941 ==> 0000000100101000001	0x26002 ==> 0010011000000000010
0x00942 ==> 0000000100101000010	0x26004 ==> 0010011000000000100
0x00944 ==> 0000000100101000100	0x26008 ==> 0010011000000001000
0x00948 ==> 0000000100101001000	0x26010 ==> 0010011000000010000
0x00950 ==> 00000000100101010000	0x26020 ==> 00100110000000100000
0x00960 ==> 00000000100101100000	0x26040 ==> 00100110000001000000
0x00981 ==> 00000000100110000001	0x26080 ==> 00100110000010000000
0x00982 ==> 00000000100110000010	0x26100 ==> 00100110000100000000
0x00984 ==> 0000000100110000100	0x26200 ==> 00100110001000000000
0x00988 ==> 0000000100110001000	0x26400 ==> 00100110010000000000
0x00990 ==> 0000000100110010000	0x26800 ==> 00100110100000000000
0x009A0 ==> 0000000100110100000	0x27000 ==> 0010011100000000000
0x009C0 ==> 0000000100111000000	0x28003 ==> 00101000000000000011
0x00A03 ==> 00000000101000000011	0x28005 ==> 00101000000000000101
0x00A05 ==> 00000000101000000101	0x28006 ==> 0010100000000000110
0x00A06 ==> 00000000101000000110	0x28009 ==> 0010100000000001001
0x00A09 ==> 00000000101000001001	0x2800A ==> 0010100000000001010
0x00A0A ==> 00000000101000001010	0x2800C ==> 0010100000000001100
0x00A0C ==> 00000000101000001100	0x28011 ==> 0010100000000010001
0x00A11 ==> 00000000101000010001	0x28012 ==> 0010100000000010010
0x00A12 ==> 00000000101000010010	0x28014 ==> 0010100000000010100
0x00A14 ==> 00000000101000010100	0x28018 ==> 0010100000000011000
0x00A18 ==> 00000000101000011000	0x28021 ==> 0010100000000100001
0x00A21 ==> 00000000101000100001	0x28022 ==> 0010100000000100010
0x00A22 ==> 00000000101000100010	0x28024 ==> 0010100000000100100

0x00A24 ==> 00000000101000100100	0x28028 ==> 0010100000000101000
0x00A28 ==> 00000000101000101000	0x28030 ==> 0010100000000110000
0x00A30 ==> 00000000101000110000	0x28041 ==> 0010100000001000001
0x00A41 ==> 00000000101001000001	0x28042 ==> 0010100000001000010
0x00A42 ==> 00000000101001000010	0x28044 ==> 0010100000001000100
0x00A44 ==> 0000000101001000100	0x28048 ==> 0010100000001001000
0x00A48 ==> 00000000101001001000	0x28050 ==> 0010100000001010000
0x00A50 ==> 00000000101001010000	0x28060 ==> 0010100000001100000
0x00A60 ==> 00000000101001100000	0x28081 ==> 0010100000010000001
0x00A81 ==> 00000000101010000001	0x28082 ==> 0010100000010000010
0x00A82 ==> 00000000101010000010	0x28084 ==> 0010100000010000100
0x00A84 ==> 00000000101010000100	0x28088 ==> 0010100000010001000
0x00A88 ==> 00000000101010001000	0x28090 ==> 0010100000010010000
0x00A90 ==> 00000000101010010000	0x280A0 ==> 0010100000010100000
0x00AA0 ==> 00000000101010100000	0x280C0 ==> 0010100000011000000
0x00AC0 ==> 00000000101011000000	0x28101 ==> 00101000000100000001
0x00B01 ==> 00000000101100000001	0x28102 ==> 00101000000100000010
0x00B02 ==> 00000000101100000010	0x28104 ==> 0010100000100000100
0x00B04 ==> 00000000101100000100	0x28108 ==> 00101000000100001000
0x00B08 ==> 00000000101100001000	0x28110 ==> 0010100000100010000
0x00B10 ==> 00000000101100010000	0x28120 ==> 00101000000100100000
0x00B20 ==> 00000000101100100000	0x28140 ==> 00101000000101000000
0x00B40 ==> 00000000101101000000	0x28180 ==> 00101000000110000000
0x00B80 ==> 00000000101110000000	0x28201 ==> 00101000001000000001
0x00C03 ==> 00000000110000000011	0x28202 ==> 00101000001000000010
0x00C05 ==> 00000000110000000101	0x28204 ==> 00101000001000000100
0x00C06 ==> 00000000110000000110	0x28208 ==> 00101000001000001000
0x00C09 ==> 00000000110000001001	0x28210 ==> 00101000001000010000
0x00C0A ==> 00000000110000001010	0x28220 ==> 00101000001000100000
0x00C0C ==> 00000000110000001100	0x28240 ==> 00101000001001000000
0x00C11 ==> 00000000110000010001	0x28280 ==> 00101000001010000000
0x00C12 ==> 00000000110000010010	0x28300 ==> 00101000001100000000
0x00C14 ==> 00000000110000010100	0x28401 ==> 00101000010000000001
0x00C18 ==> 00000000110000011000	0x28402 ==> 00101000010000000010
0x00C21 ==> 00000000110000100001	0x28404 ==> 00101000010000000100
0x00C22 ==> 00000000110000100010	0x28408 ==> 0010100001000001000

0x00C24 ==> 00000000110000100100	0x28410 ==> 00101000010000010000
0x00C28 ==> 00000000110000101000	0x28420 ==> 00101000010000100000
0x00C30 ==> 00000000110000110000	0x28440 ==> 00101000010001000000
0x00C41 ==> 00000000110001000001	0x28480 ==> 00101000010010000000
0x00C42 ==> 00000000110001000010	0x28500 ==> 00101000010100000000
0x00C44 ==> 00000000110001000100	0x28600 ==> 00101000011000000000
0x00C48 ==> 00000000110001001000	0x28801 ==> 00101000100000000001
0x00C50 ==> 00000000110001010000	0x28802 ==> 0010100010000000010
0x00C60 ==> 00000000110001100000	0x28804 ==> 0010100010000000100
0x00C81 ==> 00000000110010000001	0x28808 ==> 0010100010000001000
0x00C82 ==> 00000000110010000010	0x28810 ==> 0010100010000010000
0x00C84 ==> 00000000110010000100	0x28820 ==> 00101000100000100000
0x00C88 ==> 00000000110010001000	0x28840 ==> 00101000100001000000
0x00C90 ==> 00000000110010010000	0x28880 ==> 00101000100010000000
0x00CA0 ==> 00000000110010100000	0x28900 ==> 00101000100100000000
0x00CC0 ==> 0000000110011000000	0x28A00 ==> 0010100010100000000
0x00D01 ==> 00000000110100000001	0x28C00 ==> 0010100011000000000
0x00D02 ==> 00000000110100000010	0x29001 ==> 00101001000000000001
0x00D04 ==> 00000000110100000100	0x29002 ==> 0010100100000000010
0x00D08 ==> 00000000110100001000	0x29004 ==> 0010100100000000100
0x00D10 ==> 00000000110100010000	0x29008 ==> 0010100100000001000
0x00D20 ==> 00000000110100100000	0x29010 ==> 0010100100000010000
0x00D40 ==> 00000000110101000000	0x29020 ==> 0010100100000100000
0x00D80 ==> 00000000110110000000	0x29040 ==> 00101001000001000000
0x00E01 ==> 00000000111000000001	0x29080 ==> 00101001000010000000
0x00E02 ==> 00000000111000000010	0x29100 ==> 00101001000100000000
0x00E04 ==> 00000000111000000100	0x29200 ==> 00101001001000000000
0x00E08 ==> 00000000111000001000	0x29400 ==> 00101001010000000000
0x00E10 ==> 00000000111000010000	0x29800 ==> 00101001100000000000
0x00E20 ==> 00000000111000100000	0x2A001 ==> 0010101000000000001
0x00E40 ==> 00000000111001000000	0x2A002 ==> 0010101000000000010
0x00E80 ==> 00000000111010000000	0x2A004 ==> 0010101000000000100
0x00F00 ==> 0000000011110000000 0	0x2A008 ==> 0010101000000001000
0x01007 ==> 0000000100000000111	0x2A010 ==> 0010101000000010000
0x0100B ==> 0000000100000001011	0x2A020 ==> 0010101000000100000
0x0100D ==> 0000000100000001101	0x2A040 ==> 0010101000001000000

0x0100E ==> 0000000100000001110	0x2A080 ==> 0010101000010000000
0x01013 ==> 0000000100000010011	0x2A100 ==> 00101010000100000000
0x01015 ==> 0000000100000010101	0x2A200 ==> 00101010001000000000
0x01016 ==> 0000000100000010110	0x2A400 ==> 0010101001000000000
0x01019 ==> 0000000100000011001	0x2A800 ==> 0010101010000000000
0x0101A ==> 0000000100000011010	0x2B000 ==> 0010101100000000000
0x0101C ==> 0000000100000011100	0x2C001 ==> 0010110000000000001
0x01023 ==> 0000000100000100011	0x2C002 ==> 0010110000000000010
0x01025 ==> 0000000100000100101	0x2C004 ==> 0010110000000000100
0x01026 ==> 0000000100000100110	0x2C008 ==> 0010110000000001000
0x01029 ==> 0000000100000101001	0x2C010 ==> 0010110000000010000
0x0102A ==> 0000000100000101010	0x2C020 ==> 0010110000000100000
0x0102C ==> 0000000100000101100	0x2C040 ==> 0010110000001000000
0x01031 ==> 00000001000000110001	0x2C080 ==> 0010110000010000000
0x01032 ==> 00000001000000110010	0x2C100 ==> 00101100000100000000
0x01034 ==> 00000001000000110100	0x2C200 ==> 0010110000100000000
0x01038 ==> 00000001000000111000	0x2C400 ==> 0010110001000000000
0x01043 ==> 00000001000001000011	0x2C800 ==> 0010110010000000000
0x01045 ==> 0000000100001000101	0x2D000 ==> 0010110100000000000
0x01046 ==> 0000000100001000110	0x2E000 ==> 0010111000000000000
0x01049 ==> 00000001000001001001	0x30003 ==> 0011000000000000011
0x0104A ==> 0000000100001001010	0x30005 ==> 0011000000000000101
0x0104C ==> 0000000100001001100	0x30006 ==> 0011000000000000110
0x01051 ==> 00000001000001010001	0x30009 ==> 0011000000000001001
0x01052 ==> 00000001000001010010	0x3000A ==> 0011000000000001010
0x01054 ==> 00000001000001010100	0x3000C ==> 0011000000000001100
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0x01062 ==> 00000001000001100010	0x30014 ==> 0011000000000010100
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0x01068 ==> 00000001000001101000	0x30021 ==> 0011000000000100001
0x01070 ==> 00000001000001110000	0x30022 ==> 0011000000000100010
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0x010C8 ==> 00000001000011001000	0x30104 ==> 0011000000100000100
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0x01111 ==> 0000000100010001	0x30208 ==> 00110000001000001000
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0x01490 ==> 00000001010010010000	0x4000D ==> 0100000000000001101
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0x01580 ==> 00000001010110000000	0x40026 ==> 0100000000000100110
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0x01C80 ==> 00000001110010000000	0x40148 ==> 0100000000101001000
0x01D00 ==> 00000001110100000000	0x40150 ==> 0100000000101010000

0x01E00 ==> 00000001111000000000	0x40160 ==> 0100000000101100000
0x02007 ==> 0000001000000000111	0x40181 ==> 0100000000110000001
0x0200B ==> 0000001000000001011	0x40182 ==> 0100000000110000010
0x0200D ==> 0000001000000001101	0x40184 ==> 0100000000110000100
0x0200E ==> 0000001000000001110	0x40188 ==> 0100000000110001000
0x02013 ==> 0000001000000010011	0x40190 ==> 0100000000110010000
0x02015 ==> 0000001000000010101	0x401A0 ==> 0100000000110100000
0x02016 ==> 0000001000000010110	0x401C0 ==> 0100000000111000000
0x02019 ==> 0000001000000011001	0x40203 ==> 0100000001000000011
0x0201A ==> 0000001000000011010	0x40205 ==> 0100000001000000101
0x0201C ==> 0000001000000011100	0x40206 ==> 0100000001000000110
0x02023 ==> 0000001000000100011	0x40209 ==> 0100000001000001001
0x02025 ==> 0000001000000100101	0x4020A ==> 0100000001000001010
0x02026 ==> 0000001000000100110	0x4020C ==> 0100000001000001100
0x02029 ==> 0000001000000101001	0x40211 ==> 0100000001000010001
0x0202A ==> 0000001000000101010	0x40212 ==> 0100000001000010010
0x0202C ==> 0000001000000101100	0x40214 ==> 0100000001000010100
0x02031 ==> 0000001000000110001	0x40218 ==> 0100000001000011000
0x02032 ==> 0000001000000110010	0x40221 ==> 0100000001000100001
0x02034 ==> 0000001000000110100	0x40222 ==> 0100000001000100010
0x02038 ==> 00000010000000111000	0x40224 ==> 0100000001000100100
0x02043 ==> 0000001000001000011	0x40228 ==> 0100000001000101000
0x02045 ==> 0000001000001000101	0x40230 ==> 0100000001000110000
0x02046 ==> 0000001000001000110	0x40241 ==> 0100000001001000001
0x02049 ==> 0000001000001001001	0x40242 ==> 0100000001001000010
0x0204A ==> 0000001000001001010	0x40244 ==> 0100000001001000100
0x0204C ==> 0000001000001001100	0x40248 ==> 0100000001001001000
0x02051 ==> 00000010000001010001	0x40250 ==> 0100000001001010000
0x02052 ==> 00000010000001010010	0x40260 ==> 0100000001001100000
0x02054 ==> 00000010000001010100	0x40281 ==> 0100000001010000001
0x02058 ==> 00000010000001011000	0x40282 ==> 0100000001010000010
0x02061 ==> 00000010000001100001	0x40284 ==> 0100000001010000100
0x02062 ==> 00000010000001100010	0x40288 ==> 0100000001010001000
0x02064 ==> 00000010000001100100	0x40290 ==> 0100000001010010000
0x02068 ==> 00000010000001101000	0x402A0 ==> 0100000001010100000
0x02070 ==> 00000010000001110000	0x402C0 ==> 0100000001011000000

0x02083 ==> 00000010000010000011	0x40301 ==> 0100000001100000001
0x02085 ==> 00000010000010000101	0x40302 ==> 0100000001100000010
0x02086 ==> 00000010000110000110	0x40304 ==> 0100000001100000100
0x02089 ==> 0000001000010001001	0x40308 ==> 0100000001100001000
0x0208A ==> 00000010000010001010	0x40310 ==> 0100000001100010000
0x0208C ==> 0000001000010001100	0x40320 ==> 0100000001100100000
0x02091 ==> 00000010000010010001	0x40340 ==> 0100000001101000000
0x02092 ==> 00000010000010010010	0x40380 ==> 0100000001110000000
0x02094 ==> 00000010000010010100	0x40403 ==> 0100000010000000011
0x02098 ==> 00000010000010011000	0x40405 ==> 0100000010000000101
0x020A1 ==> 00000010000010100001	0x40406 ==> 0100000010000000110
0x020A2 ==> 00000010000010100010	0x40409 ==> 0100000010000001001
0x020A4 ==> 00000010000010100100	0x4040A ==> 0100000010000001010
0x020A8 ==> 00000010000010101000	0x4040C ==> 0100000010000001100
0x020B0 ==> 00000010000010110000	0x40411 ==> 0100000010000010001
0x020C1 ==> 00000010000011000001	0x40412 ==> 0100000010000010010
0x020C2 ==> 00000010000011000010	0x40414 ==> 0100000010000010100
0x020C4 ==> 00000010000011000100	0x40418 ==> 0100000010000011000
0x020C8 ==> 00000010000011001000	0x40421 ==> 0100000010000100001
0x020D0 ==> 00000010000011010000	0x40422 ==> 0100000010000100010
0x020E0 ==> 00000010000011100000	0x40424 ==> 0100000010000100100
0x02103 ==> 00000010000100000011	0x40428 ==> 0100000010000101000
0x02105 ==> 0000001000010000101	0x40430 ==> 0100000010000110000
0x02106 ==> 00000010000100000110	0x40441 ==> 0100000010001000001
0x02109 ==> 00000010000100001001	0x40442 ==> 0100000010001000010
0x0210A ==> 00000010000100001010	0x40444 ==> 0100000010001000100
0x0210C ==> 00000010000100001100	0x40448 ==> 0100000010001001000
0x02111 ==> 0000001000010001	0x40450 ==> 0100000010001010000
0x02112 ==> 00000010000100010010	0x40460 ==> 0100000010001100000
0x02114 ==> 00000010000100010100	0x40481 ==> 0100000010010000001
0x02118 ==> 00000010000100011000	0x40482 ==> 0100000010010000010
0x02121 ==> 00000010000100100001	0x40484 ==> 0100000010010000100
0x02122 ==> 0000001000010010010	0x40488 ==> 0100000010010001000
0x02124 ==> 00000010000100100100	0x40490 ==> 0100000010010010000
0x02128 ==> 00000010000100101000	0x404A0 ==> 0100000010010100000
0x02130 ==> 00000010000100110000	0x404C0 ==> 0100000010011000000

0x02141 ==> 00000010000101000001	0x40501 ==> 0100000010100000001
0x02142 ==> 00000010000101000010	0x40502 ==> 0100000010100000010
0x02144 ==> 00000010000101000100	0x40504 ==> 0100000010100000100
0x02148 ==> 00000010000101001000	0x40508 ==> 0100000010100001000
0x02150 ==> 00000010000101010000	0x40510 ==> 0100000010100010000
0x02160 ==> 00000010000101100000	0x40520 ==> 0100000010100100000
0x02181 ==> 00000010000110000001	0x40540 ==> 0100000010101000000
0x02182 ==> 00000010000110000010	0x40580 ==> 0100000010110000000
0x02184 ==> 00000010000110000100	0x40601 ==> 0100000011000000001
0x02188 ==> 00000010000110001000	0x40602 ==> 0100000011000000010
0x02190 ==> 00000010000110010000	0x40604 ==> 0100000011000000100
0x021A0 ==> 00000010000110100000	0x40608 ==> 0100000011000001000
0x021C0 ==> 00000010000111000000	0x40610 ==> 0100000011000010000
0x02203 ==> 00000010001000000011	0x40620 ==> 0100000011000100000
0x02205 ==> 0000001000100000101	0x40640 ==> 0100000011001000000
0x02206 ==> 0000001000100000110	0x40680 ==> 0100000011010000000
0x02209 ==> 0000001000100001001	0x40700 ==> 01000000011100000000
0x0220A ==> 0000001000100001010	0x40803 ==> 0100000010000000011
0x0220C ==> 00000010001000001100	0x40805 ==> 01000000100000000101
0x02211 ==> 0000001000100010001	0x40806 ==> 0100000010000000110
0x02212 ==> 0000001000100010010	0x40809 ==> 0100000010000001001
0x02214 ==> 0000001000100010100	0x4080A ==> 010000010000001010
0x02218 ==> 00000010001000011000	0x4080C ==> 010000010000001100
0x02221 ==> 00000010001000100001	0x40811 ==> 0100000010000010001
0x02222 ==> 00000010001000100010	0x40812 ==> 01000000100000010010
0x02224 ==> 00000010001000100100	0x40814 ==> 01000000100000010100
0x02228 ==> 00000010001000101000	0x40818 ==> 01000000100000011000
0x02230 ==> 00000010001000110000	0x40821 ==> 01000000100000100001
0x02241 ==> 00000010001001000001	0x40822 ==> 01000000100000100010
0x02242 ==> 00000010001001000010	0x40824 ==> 01000000100000100100
0x02244 ==> 00000010001001000100	0x40828 ==> 01000000100000101000
0x02248 ==> 00000010001001001000	0x40830 ==> 01000000100000110000
0x02250 ==> 00000010001001010000	0x40841 ==> 01000000100001000001
0x02260 ==> 00000010001001100000	0x40842 ==> 01000000100001000010
0x02281 ==> 00000010001010000001	0x40844 ==> 01000000100001000100
0x02282 ==> 00000010001010000010	0x40848 ==> 01000000100001001000

0x02284 ==> 00000010001010000100	0x40850 ==> 01000000100001010000
0x02288 ==> 00000010001010001000	0x40860 ==> 01000000100001100000
0x02290 ==> 00000010001010010000	0x40881 ==> 01000000100010000001
0x022A0 ==> 00000010001010100000	0x40882 ==> 01000000100010000010
0x022C0 ==> 00000010001011000000	0x40884 ==> 01000000100010000100
0x02301 ==> 00000010001100000001	0x40888 ==> 01000000100010001000
0x02302 ==> 00000010001100000010	0x40890 ==> 01000000100010010000
0x02304 ==> 00000010001100000100	0x408A0 ==> 01000000100010100000
0x02308 ==> 00000010001100001000	0x408C0 ==> 0100000100011000000
0x02310 ==> 00000010001100010000	0x40901 ==> 01000000100100000001
0x02320 ==> 00000010001100100000	0x40902 ==> 01000000100100000010
0x02340 ==> 00000010001101000000	0x40904 ==> 01000000100100000100
0x02380 ==> 00000010001110000000	0x40908 ==> 01000000100100001000
0x02403 ==> 0000001001000000011	0x40910 ==> 01000000100100010000
0x02405 ==> 0000001001000000101	0x40920 ==> 01000000100100100000
0x02406 ==> 0000001001000000110	0x40940 ==> 01000000100101000000
0x02409 ==> 0000001001000001001	0x40980 ==> 01000000100110000000
0x0240A ==> 0000001001000001010	0x40A01 ==> 01000000101000000001
0x0240C ==> 00000010010000001100	0x40A02 ==> 01000000101000000010
0x02411 ==> 00000010010000010001	0x40A04 ==> 01000000101000000100
0x02412 ==> 00000010010000010010	0x40A08 ==> 01000000101000001000
0x02414 ==> 00000010010000010100	0x40A10 ==> 0100000101000010000
0x02418 ==> 00000010010000011000	0x40A20 ==> 01000000101000100000
0x02421 ==> 00000010010000100001	0x40A40 ==> 0100000101001000000
0x02422 ==> 00000010010000100010	0x40A80 ==> 0100000101010000000
0x02424 ==> 00000010010000100100	0x40B00 ==> 0100000101100000000
0x02428 ==> 00000010010000101000	0x40C01 ==> 01000000110000000001
0x02430 ==> 00000010010000110000	0x40C02 ==> 0100000011000000010
0x02441 ==> 00000010010001000001	0x40C04 ==> 01000000110000000100
0x02442 ==> 0000001001000100010	0x40C08 ==> 01000000110000001000
0x02444 ==> 00000010010001000100	0x40C10 ==> 01000000110000010000
0x02448 ==> 00000010010001000	0x40C20 ==> 01000000110000100000
0x02450 ==> 00000010010001010000	0x40C40 ==> 01000000110001000000
0x02460 ==> 00000010010001100000	0x40C80 ==> 01000000110010000000
0x02481 ==> 00000010010010000001	0x40D00 ==> 01000000110100000000
0x02482 ==> 00000010010010000010	0x40E00 ==> 0100000011100000000

0x02484 ==> 00000010010010000100	0x41003 ==> 0100000100000000011
0x02488 ==> 00000010010010001000	0x41005 ==> 0100000100000000101
0x02490 ==> 00000010010010010000	0x41006 ==> 0100000100000000110
0x024A0 ==> 00000010010010100000	0x41009 ==> 0100000100000001001
0x024C0 ==> 00000010010011000000	0x4100A ==> 0100000100000001010
0x02501 ==> 00000010010100000001	0x4100C ==> 0100000100000001100
0x02502 ==> 00000010010100000010	0x41011 ==> 0100000100000010001
0x02504 ==> 00000010010100000100	0x41012 ==> 0100000100000010010
0x02508 ==> 00000010010100001000	0x41014 ==> 0100000100000010100
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0x02520 ==> 00000010010100100000	0x41021 ==> 0100000100000100001
0x02540 ==> 00000010010101000000	0x41022 ==> 0100000100000100010
0x02580 ==> 00000010010110000000	0x41024 ==> 0100000100000100100
0x02601 ==> 00000010011000000001	0x41028 ==> 0100000100000101000
0x02602 ==> 00000010011000000010	0x41030 ==> 01000001000000110000
0x02604 ==> 00000010011000000100	0x41041 ==> 01000001000001000001
0x02608 ==> 00000010011000001000	0x41042 ==> 0100000100001000010
0x02610 ==> 00000010011000010000	0x41044 ==> 0100000100001000100
0x02620 ==> 00000010011000100000	0x41048 ==> 01000001000001001000
0x02640 ==> 00000010011001000000	0x41050 ==> 01000001000001010000
0x02680 ==> 00000010011010000000	0x41060 ==> 01000001000001100000
0x02700 ==> 00000010011100000000	0x41081 ==> 01000001000010000001
0x02803 ==> 0000001010000000011	0x41082 ==> 01000001000010000010
0x02805 ==> 0000001010000000101	0x41084 ==> 01000001000010000100
0x02806 ==> 0000001010000000110	0x41088 ==> 01000001000010001000
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0x0280C ==> 00000010100000001100	0x410C0 ==> 01000001000011000000
0x02811 ==> 0000001010000010001	0x41101 ==> 01000001000100000001
0x02812 ==> 0000001010000010010	0x41102 ==> 01000001000100000010
0x02814 ==> 00000010100000010100	0x41104 ==> 0100000100010000100
0x02818 ==> 00000010100000011000	0x41108 ==> 0100000100010001000
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0x02822 ==> 00000010100000100010	0x41120 ==> 01000001000100100000
0x02824 ==> 00000010100000100100	0x41140 ==> 01000001000101000000
0x02828 ==> 00000010100000101000	0x41180 ==> 01000001000110000000

0x02830 ==> 00000010100000110000	0x41201 ==> 01000001001000000001
0x02841 ==> 00000010100001000001	0x41202 ==> 01000001001000000010
0x02842 ==> 00000010100001000010	0x41204 ==> 01000001001000000100
0x02844 ==> 00000010100001000	0x41208 ==> 01000001001000001000
0x02848 ==> 00000010100001001000	0x41210 ==> 01000001001000010000
0x02850 ==> 00000010100001010000	0x41220 ==> 01000001001000100000
0x02860 ==> 00000010100001100000	0x41240 ==> 01000001001001000000
0x02881 ==> 00000010100010000001	0x41280 ==> 01000001001010000000
0x02882 ==> 00000010100010000010	0x41300 ==> 01000001001100000000
0x02884 ==> 0000001010001000100	0x41401 ==> 01000001010000000001
0x02888 ==> 00000010100010001000	0x41402 ==> 01000001010000000010
0x02890 ==> 00000010100010010000	0x41404 ==> 0100000101000000100
0x028A0 ==> 00000010100010100000	0x41408 ==> 01000001010000001000
0x028C0 ==> 00000010100011000000	0x41410 ==> 01000001010000010000
0x02901 ==> 00000010100100000001	0x41420 ==> 01000001010000100000
0x02902 ==> 00000010100100000010	0x41440 ==> 01000001010001000000
0x02904 ==> 00000010100100000100	0x41480 ==> 01000001010010000000
0x02908 ==> 00000010100100001000	0x41500 ==> 01000001010100000000
0x02910 ==> 00000010100100010000	0x41600 ==> 01000001011000000000
0x02920 ==> 00000010100100100000	0x41801 ==> 01000001100000000001
0x02940 ==> 00000010100101000000	0x41802 ==> 0100000110000000010
0x02980 ==> 00000010100110000000	0x41804 ==> 0100000110000000100
0x02A01 ==> 00000010101000000001	0x41808 ==> 0100000110000001000
0x02A02 ==> 0000001010100000010	0x41810 ==> 01000001100000010000
0x02A04 ==> 00000010101000000100	0x41820 ==> 01000001100000100000
0x02A08 ==> 00000010101000001000	0x41840 ==> 01000001100001000000
0x02A10 ==> 00000010101000010000	0x41880 ==> 01000001100010000000
0x02A20 ==> 00000010101000100000	0x41900 ==> 0100000110010000000
0x02A40 ==> 00000010101001000000	0x41A00 ==> 0100000110100000000
0x02A80 ==> 00000010101010000000	0x41C00 ==> 0100000111000000000
0x02B00 ==> 00000010111100000000	0x42003 ==> 0100001000000000011
0x02C01 ==> 0000001011000000001	0x42005 ==> 0100001000000000101
0x02C02 ==> 0000001011000000010	0x42006 ==> 0100001000000000110
0x02C04 ==> 0000001011000000100	0x42009 ==> 0100001000000001001
0x02C08 ==> 00000010110000001000	0x4200A ==> 0100001000000001010
0x02C10 ==> 00000010110000010000	0x4200C ==> 0100001000000001100

0x02C20 ==> 00000010110000100000	0x42011 ==> 0100001000000010001
0x02C40 ==> 00000010110001000000	0x42012 ==> 0100001000000010010
0x02C80 ==> 00000010110010000000	0x42014 ==> 0100001000000010100
0x02D00 ==> 00000010110100000000	0x42018 ==> 0100001000000011000
0x02E00 ==> 00000010111000000000	0x42021 ==> 0100001000000100001
0x03003 ==> 0000001100000000011	0x42022 ==> 0100001000000100010
0x03005 ==> 0000001100000000101	0x42024 ==> 0100001000000100100
0x03006 ==> 0000001100000000110	0x42028 ==> 0100001000000101000
0x03009 ==> 0000001100000001001	0x42030 ==> 0100001000000110000
0x0300A ==> 0000001100000001010	0x42041 ==> 0100001000001000001
0x0300C ==> 0000001100000001100	0x42042 ==> 0100001000001000010
0x03011 ==> 0000001100000010001	0x42044 ==> 0100001000001000100
0x03012 ==> 0000001100000010010	0x42048 ==> 0100001000001001000
0x03014 ==> 0000001100000010100	0x42050 ==> 0100001000001010000
0x03018 ==> 0000001100000011000	0x42060 ==> 01000010000001100000
0x03021 ==> 0000001100000100001	0x42081 ==> 01000010000010000001
0x03022 ==> 00000011000000100010	0x42082 ==> 0100001000010000010
0x03024 ==> 00000011000000100100	0x42084 ==> 0100001000010000100
0x03028 ==> 00000011000000101000	0x42088 ==> 0100001000010001000
0x03030 ==> 00000011000000110000	0x42090 ==> 0100001000010010000
0x03041 ==> 00000011000001000001	0x420A0 ==> 0100001000010100000
0x03042 ==> 00000011000001000010	0x420C0 ==> 01000010000011000000
0x03044 ==> 00000011000001000100	0x42101 ==> 01000010000100000001
0x03048 ==> 00000011000001001000	0x42102 ==> 0100001000010000010
0x03050 ==> 00000011000001010000	0x42104 ==> 0100001000010000100
0x03060 ==> 00000011000001100000	0x42108 ==> 01000010000100001000
0x03081 ==> 00000011000010000001	0x42110 ==> 01000010000100010000
0x03082 ==> 00000011000010000010	0x42120 ==> 01000010000100100000
0x03084 ==> 00000011000010000100	0x42140 ==> 01000010000101000000
0x03088 ==> 00000011000010001000	0x42180 ==> 01000010000110000000
0x03090 ==> 00000011000010010000	0x42201 ==> 01000010001000000001
0x030A0 ==> 00000011000010100000	0x42202 ==> 0100001000100000010
0x030C0 ==> 00000011000011000000	0x42204 ==> 0100001000100000100
0x03101 ==> 00000011000100000001	0x42208 ==> 0100001000100001000
0x03102 ==> 0000001100010000010	0x42210 ==> 01000010001000010000
0x03104 ==> 00000011000100000100	0x42220 ==> 01000010001000100000

0x03108 ==> 00000011000100001000	0x42240 ==> 01000010001001000000
0x03110 ==> 00000011000100010000	0x42280 ==> 01000010001010000000
0x03120 ==> 00000011000100100000	0x42300 ==> 01000010001100000000
0x03140 ==> 00000011000101000000	0x42401 ==> 01000010010000000001
0x03180 ==> 00000011000110000000	0x42402 ==> 0100001001000000010
0x03201 ==> 00000011001000000001	0x42404 ==> 0100001001000000100
0x03202 ==> 0000001100100000010	0x42408 ==> 01000010010000001000
0x03204 ==> 00000011001000000100	0x42410 ==> 01000010010000010000
0x03208 ==> 00000011001000001000	0x42420 ==> 01000010010000100000
0x03210 ==> 00000011001000010000	0x42440 ==> 01000010010001000000
0x03220 ==> 00000011001000100000	0x42480 ==> 01000010010010000000
0x03240 ==> 00000011001001000000	0x42500 ==> 01000010010100000000
0x03280 ==> 00000011001010000000	0x42600 ==> 01000010011000000000
0x03300 ==> 00000011001100000000	0x42801 ==> 01000010100000000001
0x03401 ==> 0000001101000000001	0x42802 ==> 0100001010000000010
0x03402 ==> 0000001101000000010	0x42804 ==> 0100001010000000100
0x03404 ==> 0000001101000000100	0x42808 ==> 0100001010000001000
0x03408 ==> 00000011010000001000	0x42810 ==> 01000010100000010000
0x03410 ==> 00000011010000010000	0x42820 ==> 01000010100000100000
0x03420 ==> 00000011010000100000	0x42840 ==> 01000010100001000000
0x03440 ==> 00000011010001000000	0x42880 ==> 01000010100010000000
0x03480 ==> 00000011010010000000	0x42900 ==> 01000010100100000000
0x03500 ==> 00000011010100000000	0x42A00 ==> 01000010101000000000
0x03600 ==> 00000011011000000000	0x42C00 ==> 01000010110000000000
0x03801 ==> 0000001110000000001	0x43001 ==> 0100001100000000001
0x03802 ==> 0000001110000000010	0x43002 ==> 0100001100000000010
0x03804 ==> 0000001110000000100	0x43004 ==> 0100001100000000100
0x03808 ==> 0000001110000001000	0x43008 ==> 0100001100000001000
0x03810 ==> 00000011100000010000	0x43010 ==> 01000011000000010000
0x03820 ==> 00000011100000100000	0x43020 ==> 01000011000000100000
0x03840 ==> 00000011100001000000	0x43040 ==> 01000011000001000000
0x03880 ==> 00000011100010000000	0x43080 ==> 01000011000010000000
0x03900 ==> 0000001110010000000	0x43100 ==> 0100001100010000000
0x03A00 ==> 0000001110100000000	0x43200 ==> 0100001100100000000
0x03C00 ==> 00000011110000000000	0x43400 ==> 0100001101000000000
0x04007 ==> 0000010000000000111	0x43800 ==> 0100001110000000000

0x0400B ==> 000001000000001011	0x44003 ==> 0100010000000000011
0x0400D ==> 0000010000000001101	0x44005 ==> 0100010000000000101
0x0400E ==> 0000010000000001110	0x44006 ==> 0100010000000000110
0x04013 ==> 0000010000000010011	0x44009 ==> 0100010000000001001
0x04015 ==> 0000010000000010101	0x4400A ==> 0100010000000001010
0x04016 ==> 0000010000000010110	0x4400C ==> 0100010000000001100
0x04019 ==> 0000010000000011001	0x44011 ==> 0100010000000010001
0x0401A ==> 0000010000000011010	0x44012 ==> 0100010000000010010
0x0401C ==> 0000010000000011100	0x44014 ==> 0100010000000010100
0x04023 ==> 0000010000000100011	0x44018 ==> 0100010000000011000
0x04025 ==> 0000010000000100101	0x44021 ==> 0100010000000100001
0x04026 ==> 0000010000000100110	0x44022 ==> 0100010000000100010
0x04029 ==> 0000010000000101001	0x44024 ==> 0100010000000100100
0x0402A ==> 0000010000000101010	0x44028 ==> 0100010000000101000
0x0402C ==> 0000010000000101100	0x44030 ==> 0100010000000110000
0x04031 ==> 0000010000000110001	0x44041 ==> 0100010000001000001
0x04032 ==> 0000010000000110010	0x44042 ==> 0100010000001000010
0x04034 ==> 0000010000000110100	0x44044 ==> 0100010000001000100
0x04038 ==> 0000010000000111000	0x44048 ==> 0100010000001001000
0x04043 ==> 0000010000001000011	0x44050 ==> 0100010000001010000
0x04045 ==> 0000010000001000101	0x44060 ==> 0100010000001100000
0x04046 ==> 0000010000001000110	0x44081 ==> 0100010000010000001
0x04049 ==> 0000010000001001001	0x44082 ==> 0100010000010000010
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0x0404C ==> 0000010000001001100	0x44088 ==> 0100010000010001000
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0x04054 ==> 0000010000001010100	0x440C0 ==> 01000100000011000000
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0x04062 ==> 0000010000001100010	0x44104 ==> 0100010000100000100
0x04064 ==> 0000010000001100100	0x44108 ==> 01000100000100001000
0x04068 ==> 0000010000001101000	0x44110 ==> 01000100000100010000
0x04070 ==> 0000010000001110000	0x44120 ==> 01000100000100100000
0x04083 ==> 0000010000010000011	0x44140 ==> 01000100000101000000
0x04085 ==> 0000010000010000101	0x44180 ==> 01000100000110000000

0x04086 ==> 0000010000010000110	0x44201 ==> 01000100001000000001
0x04089 ==> 0000010000010001001	0x44202 ==> 01000100001000000010
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0x0408C ==> 0000010000010001100	0x44208 ==> 0100010000100001000
0x04091 ==> 0000010000010010001	0x44210 ==> 01000100001000010000
0x04092 ==> 0000010000010010010	0x44220 ==> 01000100001000100000
0x04094 ==> 0000010000010010100	0x44240 ==> 01000100001001000000
0x04098 ==> 0000010000010011000	0x44280 ==> 01000100001010000000
0x040A1 ==> 0000010000010100001	0x44300 ==> 01000100001100000000
0x040A2 ==> 0000010000010100010	0x44401 ==> 01000100010000000001
0x040A4 ==> 0000010000010100100	0x44402 ==> 0100010001000000010
0x040A8 ==> 0000010000010101000	0x44404 ==> 0100010001000000100
0x040B0 ==> 0000010000010110000	0x44408 ==> 01000100010000001000
0x040C1 ==> 00000100000011000001	0x44410 ==> 0100010001000010000
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0x040C8 ==> 00000100000011001000	0x44480 ==> 01000100010010000000
0x040D0 ==> 0000010000011010000	0x44500 ==> 01000100010100000000
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0x0410C ==> 00000100000100001100	0x44820 ==> 01000100100000100000
0x04111 ==> 00000100000100010001	0x44840 ==> 01000100100001000000
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0x0500A ==> 0000010100000001010	0x500C0 ==> 0101000000011000000
0x0500C ==> 0000010100000001100	0x50101 ==> 0101000000100000001
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0x06408 ==> 0000011001000001000	0x60044 ==> 0110000000001000100
0x06410 ==> 00000110010000010000	0x60048 ==> 0110000000001001000
0x06420 ==> 00000110010000100000	0x60050 ==> 0110000000001010000
0x06440 ==> 00000110010001000000	0x60060 ==> 0110000000001100000
0x06480 ==> 00000110010010000000	0x60081 ==> 0110000000010000001
0x06500 ==> 0000011001010000000	0x60082 ==> 0110000000010000010
0x06600 ==> 00000110011000000000	0x60084 ==> 0110000000010000100
0x06801 ==> 0000011010000000001	0x60088 ==> 0110000000010001000
0x06802 ==> 0000011010000000010	0x60090 ==> 0110000000010010000
0x06804 ==> 0000011010000000100	0x600A0 ==> 0110000000010100000
0x06808 ==> 0000011010000001000	0x600C0 ==> 0110000000011000000
0x06810 ==> 00000110100000010000	0x60101 ==> 0110000000100000001
0x06820 ==> 00000110100000100000	0x60102 ==> 0110000000100000010
0x06840 ==> 00000110100001000000	0x60104 ==> 0110000000100000100
0x06880 ==> 00000110100010000000	0x60108 ==> 0110000000100001000
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0x06A00 ==> 0000011010100000000	0x60120 ==> 0110000000100100000
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0x07001 ==> 0000011100000000001	0x60180 ==> 0110000000110000000
0x07002 ==> 0000011100000000010	0x60201 ==> 0110000001000000001
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0x07010 ==> 00000111000000010000	0x60208 ==> 0110000001000001000
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0x07040 ==> 00000111000001000000	0x60220 ==> 0110000001000100000
0x07080 ==> 00000111000010000000	0x60240 ==> 0110000001001000000
0x07100 ==> 0000011100010000000	0x60280 ==> 0110000001010000000

0x07200 ==> 0000011100100000000	0x60300 ==> 0110000001100000000
0x07400 ==> 0000011101000000000	0x60401 ==> 01100000010000000001
0x07800 ==> 0000011110000000000	0x60402 ==> 0110000010000000010
0x08007 ==> 0000100000000000111	0x60404 ==> 0110000001000000100
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0x0800D ==> 0000100000000001101	0x60410 ==> 01100000010000010000
0x0800E ==> 0000100000000001110	0x60420 ==> 01100000010000100000
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0x08085 ==> 0000100000010000101	0x62020 ==> 0110001000000100000
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0x0820C ==> 00001000001000001100	0x80007 ==> 1000000000000000111
0x08211 ==> 00001000001000010001	0x8000B ==> 1000000000000001011
0x08212 ==> 00001000001000010010	0x8000D ==> 1000000000000001101
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0x08218 ==> 00001000001000011000	0x80013 ==> 1000000000000010011
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0x08241 ==> 00001000001001000001	0x80023 ==> 1000000000000100011
0x08242 ==> 00001000001001000010	0x80025 ==> 1000000000000100101
0x08244 ==> 00001000001001000100	0x80026 ==> 1000000000000100110
0x08248 ==> 00001000001001001000	0x80029 ==> 1000000000000101001
0x08250 ==> 00001000001001010000	0x8002A ==> 1000000000000101010
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0x08284 ==> 00001000001010000100	0x80034 ==> 1000000000000110100
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0x08D00 ==> 00001000110100000000	0x80418 ==> 1000000010000011000
0x08E00 ==> 00001000111000000000	0x80421 ==> 1000000010000100001
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0x09005 ==> 0000100100000000101	0x80424 ==> 1000000010000100100
0x09006 ==> 0000100100000000110	0x80428 ==> 1000000010000101000
0x09009 ==> 0000100100000001001	0x80430 ==> 1000000010000110000
0x0900A ==> 0000100100000001010	0x80441 ==> 1000000010001000001
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0x09011 ==> 0000100100000010001	0x80444 ==> 1000000010001000100
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0x09180 ==> 00001001000110000000	0x80805 ==> 1000000010000000101
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0x09202 ==> 0000100100100000010	0x80809 ==> 1000000010000001001
0x09204 ==> 0000100100100000100	0x8080A ==> 1000000010000001010
0x09208 ==> 0000100100100001000	0x8080C ==> 10000000100000001100
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0x09280 ==> 00001001001010000000	0x80818 ==> 10000000100000011000
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0x09420 ==> 00001001010000100000	0x80842 ==> 10000000100001000010
0x09440 ==> 00001001010001000000	0x80844 ==> 10000000100001000100
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0x09500 ==> 00001001010100000000	0x80850 ==> 10000000100001010000
0x09600 ==> 0000100101100000000	0x80860 ==> 10000000100001100000
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0x09802 ==> 0000100110000000010	0x80882 ==> 10000000100010000010
0x09804 ==> 0000100110000000100	0x80884 ==> 10000000100010000100
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0x09840 ==> 00001001100001000000	0x808C0 ==> 1000000100011000000
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0x09900 ==> 0000100110010000000	0x80902 ==> 10000000100100000010
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0x09C00 ==> 0000100111000000000	0x80908 ==> 10000000100100001000
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0x0A005 ==> 0000101000000000101	0x80920 ==> 10000000100100100000
0x0A006 ==> 0000101000000000110	0x80940 ==> 1000000100101000000
0x0A009 ==> 0000101000000001001	0x80980 ==> 10000000100110000000
0x0A00A ==> 0000101000000001010	0x80A01 ==> 10000000101000000001
0x0A00C ==> 0000101000000001100	0x80A02 ==> 10000000101000000010
0x0A011 ==> 0000101000000010001	0x80A04 ==> 10000000101000000100
0x0A012 ==> 0000101000000010010	0x80A08 ==> 10000000101000001000
0x0A014 ==> 0000101000000010100	0x80A10 ==> 10000000101000010000
0x0A018 ==> 0000101000000011000	0x80A20 ==> 10000000101000100000
0x0A021 ==> 0000101000000100001	0x80A40 ==> 1000000101001000000
0x0A022 ==> 0000101000000100010	0x80A80 ==> 1000000101010000000
0x0A024 ==> 0000101000000100100	0x80B00 ==> 1000000101100000000
0x0A028 ==> 0000101000000101000	0x80C01 ==> 10000000110000000001
0x0A030 ==> 0000101000000110000	0x80C02 ==> 1000000011000000010
0x0A041 ==> 0000101000001000001	0x80C04 ==> 10000000110000000100
0x0A042 ==> 0000101000001000010	0x80C08 ==> 10000000110000001000
0x0A044 ==> 0000101000001000100	0x80C10 ==> 10000000110000010000
0x0A048 ==> 0000101000001001000	0x80C20 ==> 10000000110000100000
0x0A050 ==> 0000101000001010000	0x80C40 ==> 10000000110001000000
0x0A060 ==> 00001010000001100000	0x80C80 ==> 10000000110010000000
0x0A081 ==> 00001010000010000001	0x80D00 ==> 10000000110100000000
0x0A082 ==> 00001010000010000010	0x80E00 ==> 10000000111000000000
0x0A084 ==> 0000101000010000100	0x81003 ==> 1000000100000000011
0x0A088 ==> 0000101000010001000	0x81005 ==> 1000000100000000101
0x0A090 ==> 0000101000010010000	0x81006 ==> 1000000100000000110
0x0A0A0 ==> 00001010000010100000	0x81009 ==> 1000000100000001001
0x0A0C0 ==> 00001010000011000000	0x8100A ==> 1000000100000001010
0x0A101 ==> 00001010000100000001	0x8100C ==> 1000000100000001100
0x0A102 ==> 00001010000100000010	0x81011 ==> 1000000100000010001
0x0A104 ==> 00001010000100000100	0x81012 ==> 1000000100000010010
0x0A108 ==> 00001010000100001000	0x81014 ==> 1000000100000010100
0x0A110 ==> 00001010000100010000	0x81018 ==> 1000000100000011000
0x0A120 ==> 00001010000100100000	0x81021 ==> 1000000100000100001
0x0A140 ==> 00001010000101000000	0x81022 ==> 1000000100000100010

0x0A180 ==> 00001010000110000000	0x81024 ==> 1000000100000100100
0x0A201 ==> 00001010001000000001	0x81028 ==> 1000000100000101000
0x0A202 ==> 0000101000100000010	0x81030 ==> 10000001000000110000
0x0A204 ==> 00001010001000000100	0x81041 ==> 10000001000001000001
0x0A208 ==> 0000101000100001000	0x81042 ==> 1000000100001000010
0x0A210 ==> 00001010001000010000	0x81044 ==> 10000001000001000100
0x0A220 ==> 00001010001000100000	0x81048 ==> 10000001000001001000
0x0A240 ==> 00001010001001000000	0x81050 ==> 10000001000001010000
0x0A280 ==> 00001010001010000000	0x81060 ==> 10000001000001100000
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0x0A401 ==> 00001010010000000001	0x81082 ==> 10000001000010000010
0x0A402 ==> 0000101001000000010	0x81084 ==> 10000001000010000100
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0x0A408 ==> 0000101001000001000	0x81090 ==> 10000001000010010000
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0x0A500 ==> 00001010010100000000	0x81104 ==> 10000001000100000100
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0x0A802 ==> 0000101010000000010	0x81120 ==> 10000001000100100000
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0x0A900 ==> 00001010100100000000	0x81210 ==> 10000001001000010000
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0x0B001 ==> 00001011000000000001	0x81280 ==> 10000001001010000000
0x0B002 ==> 0000101100000000010	0x81300 ==> 10000001001100000000
0x0B004 ==> 0000101100000000100	0x81401 ==> 10000001010000000001
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0x0C003 ==> 0000110000000000011	0x81801 ==> 10000001100000000001
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0x0C00A ==> 0000110000000001010	0x81810 ==> 10000001100000010000
0x0C00C ==> 0000110000000001100	0x81820 ==> 10000001100000100000
0x0C011 ==> 0000110000000010001	0x81840 ==> 10000001100001000000
0x0C012 ==> 0000110000000010010	0x81880 ==> 10000001100010000000
0x0C014 ==> 0000110000000010100	0x81900 ==> 10000001100100000000
0x0C018 ==> 0000110000000011000	0x81A00 ==> 10000001101000000000
0x0C021 ==> 0000110000000100001	0x81C00 ==> 10000001110000000000
0x0C022 ==> 0000110000000100010	0x82003 ==> 1000001000000000011
0x0C024 ==> 0000110000000100100	0x82005 ==> 1000001000000000101
0x0C028 ==> 0000110000000101000	0x82006 ==> 1000001000000000110
0x0C030 ==> 0000110000000110000	0x82009 ==> 1000001000000001001
0x0C041 ==> 0000110000001000001	0x8200A ==> 1000001000000001010
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0x0C044 ==> 0000110000001000100	0x82011 ==> 1000001000000010001
0x0C048 ==> 0000110000001001000	0x82012 ==> 1000001000000010010
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0x0C060 ==> 0000110000001100000	0x82018 ==> 1000001000000011000
0x0C081 ==> 00001100000010000001	0x82021 ==> 1000001000000100001
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0x0C084 ==> 0000110000010000100	0x82024 ==> 1000001000000100100
0x0C088 ==> 0000110000010001000	0x82028 ==> 1000001000000101000
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0x0C0A0 ==> 00001100000010100000	0x82041 ==> 1000001000001000001
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0x0C201 ==> 00001100001000000001	0x82090 ==> 1000001000010010000
0x0C202 ==> 00001100001000000010	0x820A0 ==> 1000001000010100000
0x0C204 ==> 00001100001000000100	0x820C0 ==> 10000010000011000000
0x0C208 ==> 0000110000100001000	0x82101 ==> 10000010000100000001
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0x0C804 ==> 0000110010000000100	0x82402 ==> 1000001001000000010
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0x0C880 ==> 00001100100010000000	0x82440 ==> 10000010010001000000
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0x0D020 ==> 0000110100000100000	0x82820 ==> 10000010100000100000
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0x10016 ==> 000100000000010110	0x84014 ==> 1000010000000010100
0x10019 ==> 000100000000011001	0x84018 ==> 1000010000000011000
0x1001A ==> 000100000000011010	0x84021 ==> 1000010000000100001
0x1001C ==> 000100000000011100	0x84022 ==> 1000010000000100010

0x10023 ==> 000100000000100011	0x84024 ==> 1000010000000100100
0x10025 ==> 000100000000100101	0x84028 ==> 1000010000000101000
0x10026 ==> 000100000000100110	0x84030 ==> 1000010000000110000
0x10029 ==> 000100000000101001	0x84041 ==> 1000010000001000001
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0x1002C ==> 000100000000101100	0x84044 ==> 1000010000001000100
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0x100C8 ==> 0001000000011001000	0x84801 ==> 1000010010000000001
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0x100E0 ==> 0001000000011100000	0x84804 ==> 1000010010000000100
0x10103 ==> 0001000000100000011	0x84808 ==> 1000010010000001000
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0x10188 ==> 0001000000110001000	0x86010 ==> 1000011000000010000
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0x10406 ==> 0001000001000000110	0x88120 ==> 1000100000100100000
0x10409 ==> 0001000001000001001	0x88140 ==> 1000100000101000000
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0x10428 ==> 00010000010000101000	0x88300 ==> 10001000001100000000
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0x10448 ==> 00010000010001001000	0x88410 ==> 10001000010000010000
0x10450 ==> 00010000010001010000	0x88420 ==> 10001000010000100000
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0x10482 ==> 00010000010010000010	0x88500 ==> 10001000010100000000
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0x10806 ==> 0001000010000000110	0x8A001 ==> 1000101000000000001
0x10809 ==> 0001000010000001001	0x8A002 ==> 1000101000000000010
0x1080A ==> 0001000010000001010	0x8A004 ==> 1000101000000000100
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0x10821 ==> 0001000010000100001	0x8A100 ==> 10001010000100000000
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0x10882 ==> 00010000100010000010	0x8C080 ==> 10001100000010000000
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0x11600 ==> 00010001011000000000	0x92004 ==> 1001001000000000100
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0x14044 ==> 0001010000001000100	0xA1002 ==> 1010000100000000010
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0x14120 ==> 00010100000100100000	0xA2020 ==> 1010001000000100000
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0x15010 ==> 0001010100000010000	0xB0001 ==> 101100000000000000001
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0x15080 ==> 00010101000010000000	0xB0008 ==> 1011000000000001000
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0x15200 ==> 0001010100100000000	0xB0020 ==> 1011000000000100000
0x15400 ==> 0001010101000000000	0xB0040 ==> 1011000000001000000
0x15800 ==> 0001010110000000000	0xB0080 ==> 1011000000010000000

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0x16004 ==> 0001011000000000100	0xB0400 ==> 10110000010000000000
0x16008 ==> 0001011000000001000	0xB0800 ==> 10110000100000000000
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0x16020 ==> 0001011000000100000	0xB2000 ==> 101100100000000000000
0x16040 ==> 00010110000001000000	0xB4000 ==> 101101000000000000000
0x16080 ==> 00010110000010000000	0xB8000 ==> 101110000000000000000
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0x16200 ==> 0001011000100000000	0xC0005 ==> 1100000000000000101
0x16400 ==> 0001011001000000000	0xC0006 ==> 1100000000000000110
0x16800 ==> 0001011010000000000	0xC0009 ==> 1100000000000001001
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Replacement Sheet

While several illustrative embodiments of the invention have been shown and described, numerous variations and alternative embodiments will occur to those skilled in the art. Such variations and alternative embodiments are contemplated, and can be made without departing from the scope of the invention as defined in the appended claims. As used in this specification and the appended claims, the singular forms "a," "an," and "the" include plural referents unless the content clearly dictates otherwise. The term "plurality" includes two or more referents unless the content clearly dictates otherwise. Unless defined otherwise, all technical and scientific terms used herein have the same meaning as commonly understood by one of ordinary skill in the art to which the disclosure pertains.

The foregoing detailed description of exemplary and preferred embodiments is presented for purposes of illustration and disclosure in accordance with the requirements of the law. It is not intended to be exhaustive nor to limit the invention to the precise form(s) described, but only to enable others skilled in the art to understand how the invention may be suited for a particular use or implementation. The possibility of modifications and variations will be apparent to practitioners skilled in the art. No limitation is intended by the description of exemplary embodiments which may have included tolerances, feature dimensions, specific operating conditions, engineering specifications, or the like, and which may vary between implementations or with changes to the state of the art, and no limitation should be implied therefrom. Applicant has made this disclosure with respect to the current state of the art, but also contemplates advancements and that adaptations in the future may take into consideration of those advancements, namely in accordance with the then current state of the art. It is intended that the scope of the invention be defined by the Claims as written and equivalents as applicable.

Reference to a claim element in the singular is not intended to mean "one and only one" unless explicitly so stated. Moreover, no element, component, nor method or process step in this disclosure is intended to be dedicated to the public regardless of whether the element, component, or step is explicitly recited in the claims. No claim element herein is to be construed under the provisions of 35 U.S.C. Sec. 112, sixth paragraph, unless the element is expressly recited using the phrase "means for. . ." and no method or process step herein is to be construed under those provisions unless the step, or steps, are expressly recited using the phrase "step(s) for. . .".

What is claimed is:

1. A network comprising: two or more devices, wherein a first device of the two or more devices is configured to provide data to a second device of the two or more devices.

ABSTRACT

A network with two or more devices, wherein a first device of the two or more devices is configured to provide data to a second device of the two or more devices.